VOICE SYNTHESIZER

DESCRIPTION

The MEA8000 is a 24-pin N-MOS integrated circuit for generating good quality speech from digital code with a programmable bit rate. The circuit is primarily intended for applications in microprocessor controlled systems, where the speech code is stored separately in a Read-Only Memory.

Features

- Interfaces easily to most popular microprocessors and microcomputers.
- 8-bit wide data bus. • 32-bit wide data buffer holding speech frame codes.
- Digital filter of 8th order with 3 programmable formant frequencies, one fixed formant frequency, and 4 programmable formant bandwidths.
- Programmable amplitudes. • Programmable duration of each frame; 8, 16, 32, or 64 milliseconds.
- Synthesis occupies less than 1% of control processor time.
- Capable of sophisticated unvoiced sound generation. • Minimal external audio filter requirement.
- Crystal controlled oscillator or external (TTL) clock. • Single +5 V power supply.

QUICK REFERENCE DATA

Supply voltage	V_{DD}	nom.	5	V
Supply current (no audio load)	I_{DD}	typ.	30	mA
Operating ambient temperature range	T_{amb}		0 to +70	°C

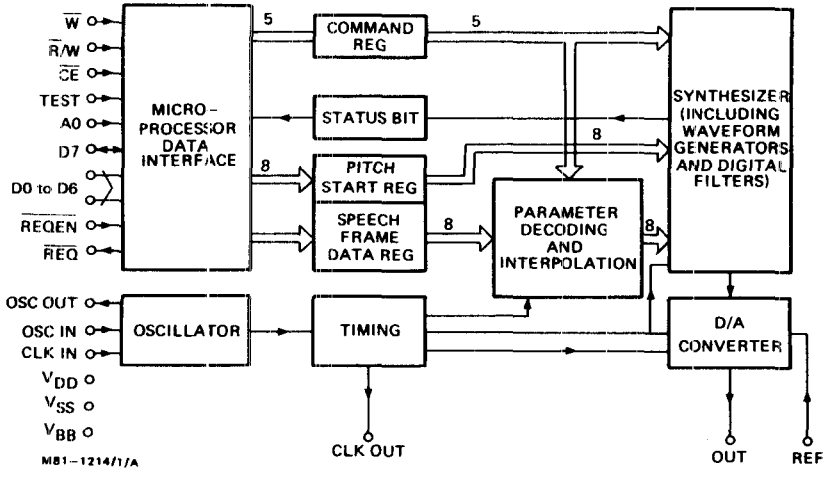


Fig.1 Block diagram

PACKAGE OUTLINE

24-lead DIL; plastic (SOT-101A)

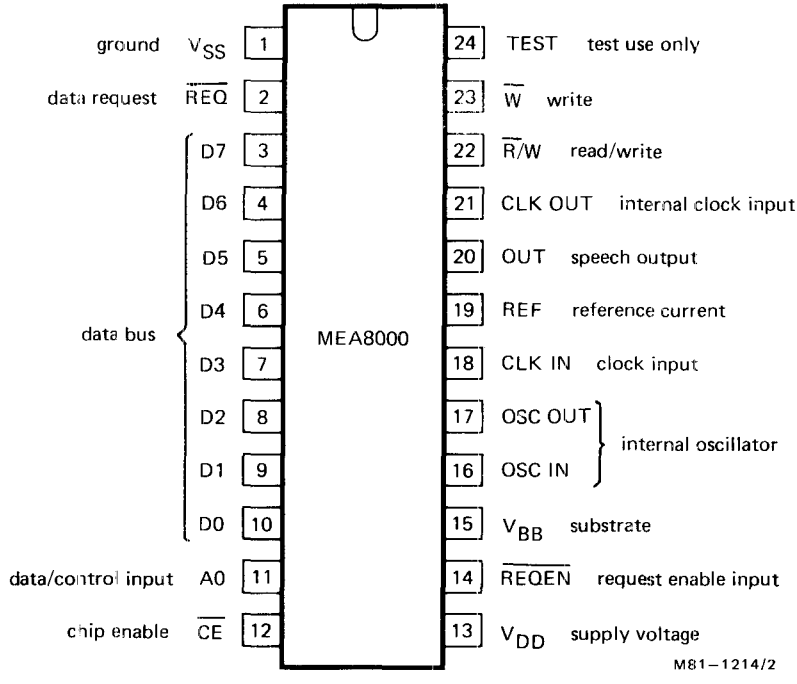


Fig.2 Pinning diagram

FUNCTIONAL PIN DESCRIPTION (Pin number)

Control

D0 to D7	(10 to 3)	Data bus to which command or speech can be written
D7	(3)	Data port via which the status can be read.
$\overline{CE}$	(12)	Chip enable (chip select).
$\overline{W}$	(23)	Write
$\overline{R}/W$	(22)	Read/Write.

These control signals allow connection to most microcomputers or microprocessors (see timing diagrams).

A0	(11)	Data/control input. Discriminates between speech code input buffer (A0 = '0') and command register (A0 = '1') during a 'write' operation.
$\overline{REQ}$	(2)	Data request (open drain output). Output signal which follows the inverse of the status REQ bit, but only if enabled by either the ROE bit in the command register or the external REQEN pin.
$\overline{REQEN}$	(14)	Request enable input. $\overline{REQEN}$ ='0' enables the status REQ bit to appear inverted on the $\overline{REQ}$ output, independent of the status of the command register.

Timing

OSC IN	(16)	Connections for internal clock oscillator. Nominal crystal 3.84 MHz.
OSC OUT	(17)	
CLK IN	(18)	Clock input for external clock, TTL compatible, 3.84 MHz.
CLK OUT	(21)	A buffered output of the internal clock cycle (= CLK divided by 3). May be used as a 1.28 MHz clock, for a microprocessor, for example.

Output

REF	(19)	Input pin for biasing the audio output level. This reference current can be derived from a resistor to the positive supply.
OUT	(20)	Speech output. This output is a 64 kHz pulse, modulated in both width and amplitude. It is configured as a current sink with a saturating voltage of about 3 V.

Supply

V_{DD}	(13)	Single supply voltage. Nominally 5 V, but battery operation is also possible.
V_{SS}	(1)	Ground.
V_{BB}	(15)	Substrate. Should be grounded.
TEST	(24)	Used for testing purposes. Changes other pin functions. Must be tied to ground for user operation.

DEVELOPMENT SAMPLE DATA

HANDLING

Inputs and outputs are protected against electrostatic charge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see 'Handling MOS Devices').

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC134).

		min.	max.	
Supply voltage	V_{DD}	−0.5	7	V
Voltage on any pin with respect to V_{SS}	V_I	−0.5	7	V
Output voltage on pins 2 and 20	$V_{\overline{REQ}}$, V_{OUT}	−	15	V
Storage temperature range	T_{stg}	−20 to +125		°C
Operating ambient temperature range	T_{amb}	0 to +70		°C

CHARACTERISTICS

T_{amb} = 25 °C ; V_{DD} = 5 V, unless otherwise stated. All voltages referenced to V_{SS}.

		min.	typ.	max.	
Supply voltage (note 1)	V_{DD}	4.5	5.0	5.5	V
Supply current (no audio load)	I_{DD}	−	30	50	mA
Inputs					
D0 to D7, A0, $\overline{CE}$ $\overline{W}$ R/$\overline{W}$ $\overline{REQEN}$, CLK IN					
Input voltage HIGH	V_{IH}	2.0	−	V_{DD}	V
Input voltage LOW	V_{IL}	−0.5	−	0.8	V
Input leakage current (note 2)	I_{IR}	−	−	10	μA
Input capacitance	C_I	−	−	7	pF
Outputs					
D7 (I/O), CLK OUT					
Output voltage HIGH ($-I_{OH}$ = 100 μA)	V_{OH}	2.4	−	−	V
Output voltage LOW (I_{OL} = 1.6 mA)	V_{OL}	−	−	0.4	V
Output load capacitance	C_L	−	−	50	pF
$\overline{REQ}$					
Output voltage HIGH (open drain)	V_{OH}	−	−	13.2	V
Output voltage LOW (I_{OL} = 1.6 mA)	V_{OL}	−	−	0.4	V
Output load capacitance	C_L	−	−	50	pF

		min.	typ.	max.	
Audio output					
Reference current (pin 19) (note 8)	I_{REF}	–	–	0.3	mA
Output current (peak) (pin 20)	I_{OUT}				
(I_{REF} = 0 mA)		–	100	–	μA
(I_{REF} = 0.1 mA)			1.7	–	mA
(I_{REF} = 0.3 mA)		–	5	–	mA
V_{OUT} (pin 20) for linear operation (note 3) (I_{REF} = 0.1 mA)	V_{OUT}	2.5	–	13.2	V
Oscillator					
Crystal frequency (internal)	f_{XTAL}	–	3.84	4.00	MHz
Clock frequency (external)	f_{CLK}	–	3.84	4.00	MHz
TIMING CHARACTERISTICS (note 4) (Figs. 6 and 7)					
Write enable	t_{WR}	200	–	–	ns
Address set-up	t_{AS}	30	–	–	ns
Address hold	t_{AH}	30	–	–	ns
Data set-up for write	t_{DS}	150	–	–	ns
Data hold for write	t_{DH}	30	–	–	ns
Request hold (note 5)	t_{RH}	–	–	350	ns
Request next (clock frequency = 3.84 MHz) (note 6)	t_{RN}	–	–	3	μs
Read enable	t_{RD}	200	–	–	ns
Data delay for read (note 7)	t_{DD}	–	–	150	ns
Data floating for read (note 7)	t_{DF}	–	–	150	ns
Request valid before write	t_{RV}	0	–	–	ns
Request output enable response	t_{ROE}	–	–	350	ns
Control set-up	t_{CS}	–	–	20	ns
Control hold	t_{CH}	–	–	20	ns

DEVELOPMENT SAMPLE DATA

Notes

1. The circuit will continue to operate from a supply of up to 6.5 V, but without necessarily meeting the specification.
2. This is also valid for V_{DD} = 0 V.
3. This permits connection of the output load to a supply higher than that supplying the synthesizer.
4. Timing reference level is 1.5 V.
5. An external pull up resistor is required, as this is an open drain output. The time (t_{RH}) to reach 2.0 V is specified at a load to 5 V of 3.3 kΩ and 50 pF.
6. Between two data write operations of one speech frame.
7. Levels greater than 2.0 V for a '1' or less than 0.8 V for a '0' are reached with a load of one TTL input and 50 pF.
8. Typical voltage level at the REF pin is 2.5 V.

OPERATION PRINCIPLE

The MEA8000 has been designed for the vocal tract modelling technique of voice synthesis. If speech quality acceptable for consumer and most industrial applications is required then this method yields the lowest possible bit rates.
The principle is illustrated in Fig.3, which shows an electronic model of the human vocal tract. A mixture of a periodic signal (representing the pitch in the original speech) and an aperiodic signal (representing the noise of the speech) is fed to a series of resonators. Every resonator makes up one more or less pronounced peak in the frequency spectrum, in accordance with one of the formants in the original speech, and is controlled by two parameters, one for the resonance frequency and one for the bandwidth. The output of this system is defined by the pitch frequency, the amplitude values and the resonator settings. By periodic updating of all parameters one can make a good replica of the speech.

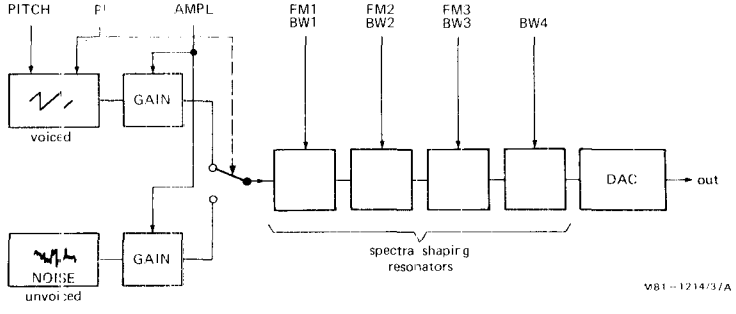


Fig.3 Electronic model of human vocal tract.

OPERATION

Speech is generated by suitable filtering of a relatively low frequency sawtooth waveform for voiced sounds or of random noise for unvoiced sounds.
New parameters for both the digital waveform generator and the digital filter are supplied to the synthesizer in coded groups of 4 bytes via the data bus. The code group also contains the duration of the next speech frame to be produced, (8, 16, 32 or 64 ms).
The output sample rate is 64 kHz or 8 times the internal sample rate with linear interpolation in between. This greatly reduces the need for an external analogue output filter.

Modes of operation.

1. STOP mode: characterised by a silent output and the status REQ bit set to '1'. This mode is entered from power up or by STOP command. The mode is entered automatically if at the end of an active speech frame the next four parameter bytes are not yet received while the CONT bit in the command register is a '0'. In the latter case the final speech frame will be repeated once but with a decaying amplitude and the same pitch.
2. ACTIVE mode: a speech sample is being produced.
3. CONTINUOUS mode: entered if an active speech frame is finished and new data is not supplied in time while the CONT bit in the command register is a '1'. The synthesizer will repeat the last speech frame indefinitely until all four new data bytes are received, or a STOP command, or a reset of the CONT bit.

Speech code input buffer

Speech code is written to the synthesizer when $\overline{CE}$ and $\overline{W}$ are both '0', while $\overline{R}/W$ = '1' and A0 = '0'. Also the status REQ bit must read a '1', otherwise the synthesizer is still busy and will not react to a data write operation.

Starting from the STOP mode, the first data will be interpreted as a starting value for the Pitch. Thereafter every four successive data bytes are treated as a group of speech code.

The coded speech frame format is shown in Fig.4.

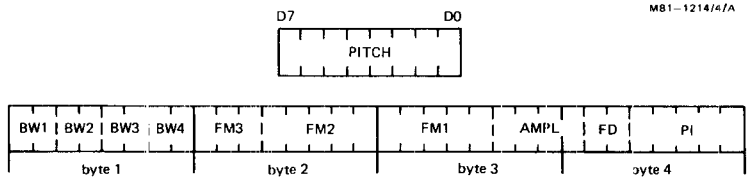


Fig.4 Format of coded speech frame

Code	Bits	Parameter
Pitch	8	Initial value for pitch
FD	2	Speech frame duration
PI	5	Pitch increment (rate of change) or noise selection
AMPL	4	Amplitude
FM1	5	Frequency of 1st formant
FM2	5	Frequency of 2nd formant
FM3	3	Frequency of 3rd formant
FM4	0	Frequency of 4th formant (fixed)
BW1	2	Bandwidth of 1st formant
BW2	2	Bandwidth of 2nd formant
BW3	2	Bandwidth of 3rd formant
BW4	2	Bandwidth of 4th formant

During each data write operation, the status REQ bit will be cleared to '0'. It appears within a few microseconds, asking for next byte of the group.

Request for the first byte of the next group always appears shortly after the beginning of the current speech frame, and all four bytes must be provided before it finishes. This leaves the control circuit (e.g. microprocessor) enough time to use polling, instead of interrupts, as the minimum time of a speech frame is 8 ms.

When in the STOP mode the synthesizer will commence producing sound after receipt of 1 + 4 bytes.

Status bit

The status bit is accessed at $\overline{CE}$ = $\overline{R}$/W = '0'

The states of $\overline{W}$ and A0 are arbitrary

Pin D7 reveals the request for a (next) speech code byte: '0' = busy, '1' = request for data.

Command register

A command is written to the synthesizer at $\overline{CE}$ = $\overline{W}$ = '0' while A0 = $\overline{R}$/W = '1'.

D7	D6	D5	D4	D3	D2	D1	D0
			STOP	CONT enable	CONT	ROE enable	ROE
NOT USED			'0' = INVALID '1' = STOP	00 = INVALID 01 = INVALID 10 = SLOW STOP 11 = CONTINUE		00 = INVALID 01 = INVALID 10 = DISABLE $\overline{REQ}$ OUTPUT 11 = ENABLE $\overline{REQ}$ OUTPUT	

STOP results in an immediate reset of the synthesizer to the STOP mode. The ROE and CONT are not affected by this command.

CONT Continuous mode. This bit can be set or cleared only if the corresponding CONT enable bit is programmed as a '1'. In the continuous mode the synthesizer will not revert to the STOP mode if all four parameters are not received before the end of the current speech frame, but repeat it indefinitely.

If CONT = '0' the last frame will be repeated once with decaying amplitude and the same pitch before the stop mode is entered.

ROE Request Output Enable. This bit can be set or cleared only if the corresponding ROE enable bit is a '1'. ROE determines whether the request in the status bit appears on the REQ pin. Note: the same can be achieved by connecting the $\overline{REQEN}$ pin (request enable) to a '0'.

After power on, the command register bits CONT and ROE will both be zero. Thus power on equals the command 00011010 = 1 A (hexadecimal).

Control signals

With the three control signals $\overline{CE}$, $\overline{W}$ and $\overline{R}$/W the synthesizer is made compatible with most popular microprocessors and microcomputers.

$\overline{CE}$	$\overline{W}$	$\overline{R}$/W	A0	Operation
0	0	1	0	WRITE DATA
0	0	1	1	WRITE COMMAND
0	X	0	X	READ STATUS
0	1	1	X	THREE-STATE DATA BUS
1	X	X	X	THREE-STATE DATA BUS

Power supply

During (slow) power up or power down the circuit will not produce any spurious sound.
As soon as the supply is high enough for reliable operation, the circuit will be in the STOP mode with ROE = CONT = '0'.

Timing diagrams

The control signals $\overline{CE}$, R/$\overline{W}$ and $\overline{W}$ have been specified to enable easy interface to most microprocessors and microcomputers. For instance with connection to an MAB8048 microcomputer the R/$\overline{W}$ and $\overline{W}$ inputs can be used as the $\overline{RD}$ and $\overline{WR}$ strobe inputs

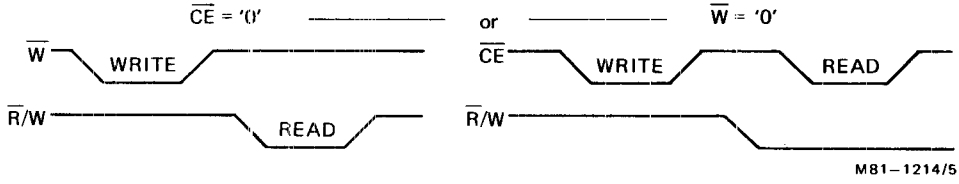


Fig.5 Typical connnection of control signals

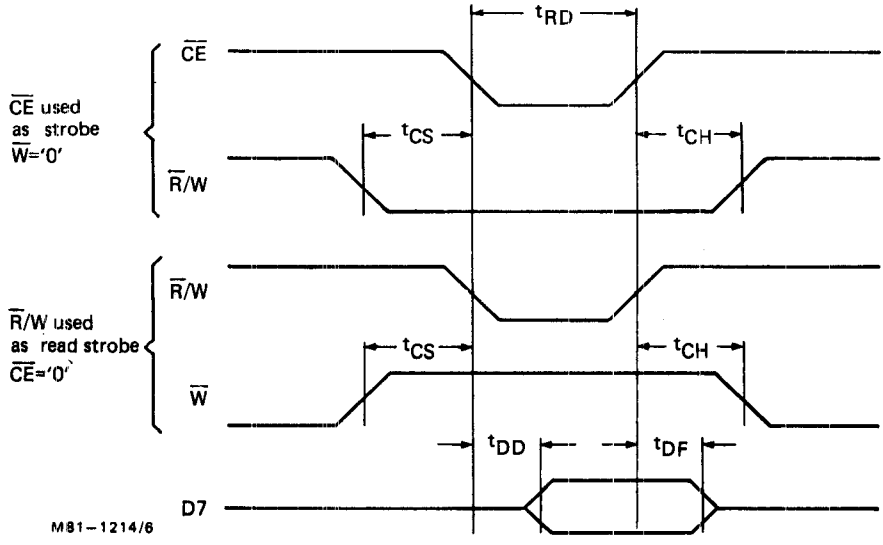


Fig.6 Read timing

Note: Address input A0 is a don't care.
Data bits D0 to D6 remain floating.

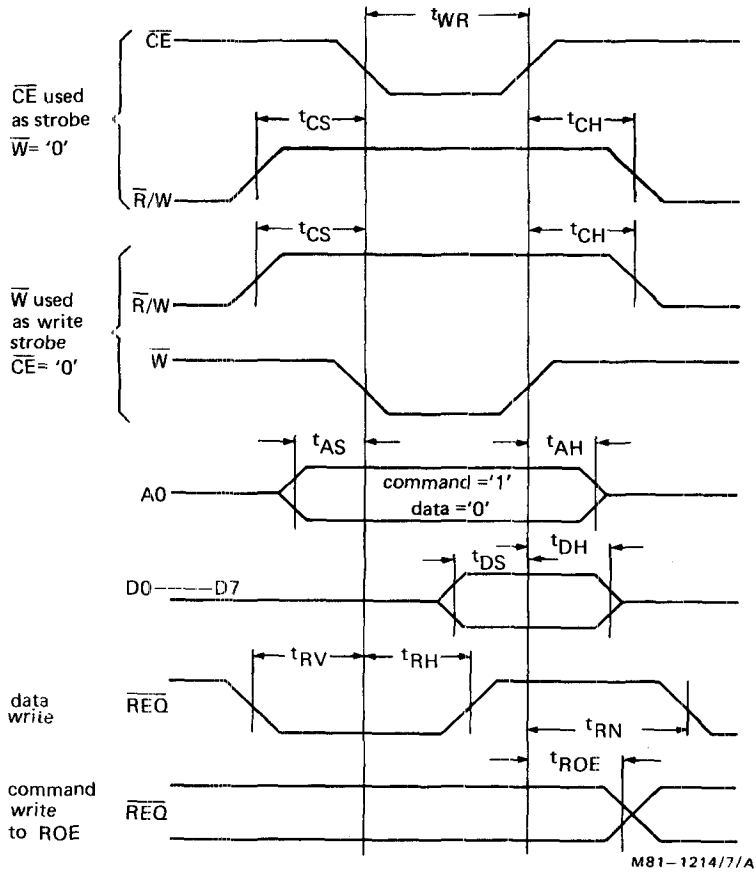
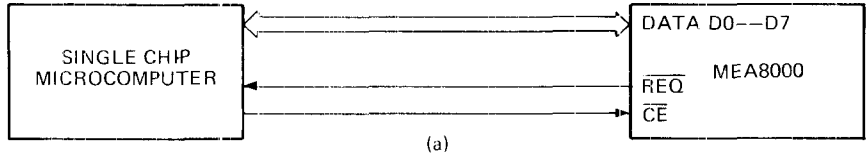
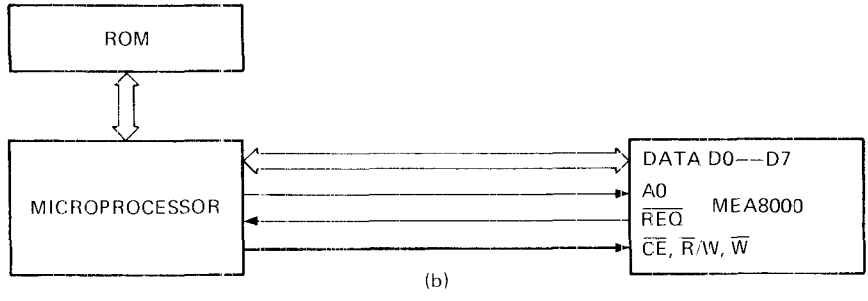


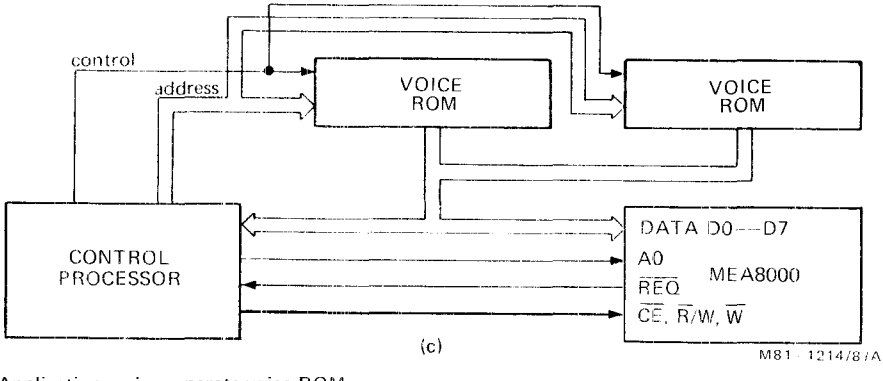
Fig.7 Write timing



a. Minimal system of single chip microcomputer with voice ROM on board.



b. MEA8000 as a microprocessor peripheral



c. Applications using separate voice ROMs.

Fig.8 Typical application configurations

DEVELOPMENT SAMPLE DATA

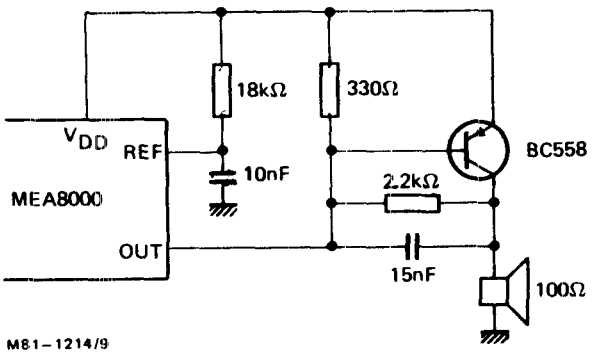


Fig.9 Typical output configuration

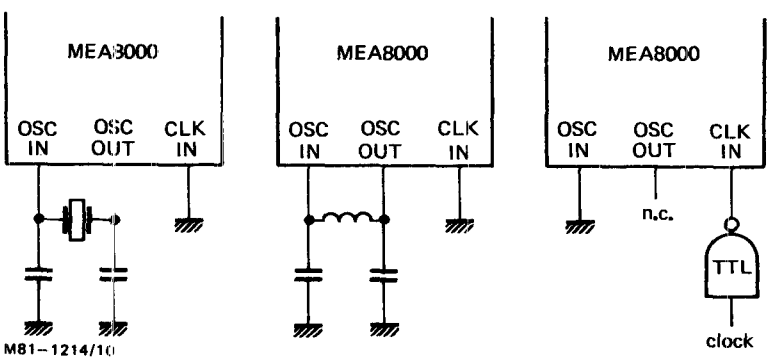
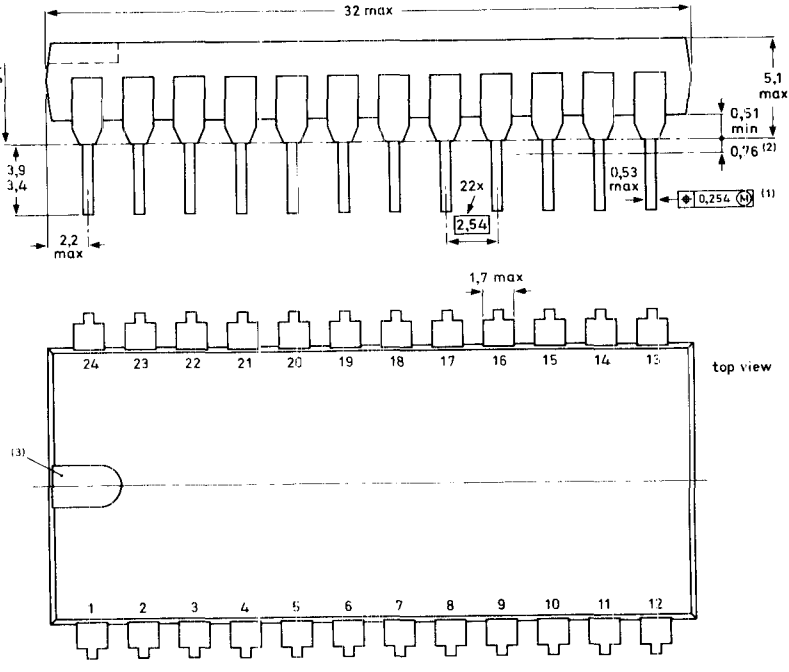
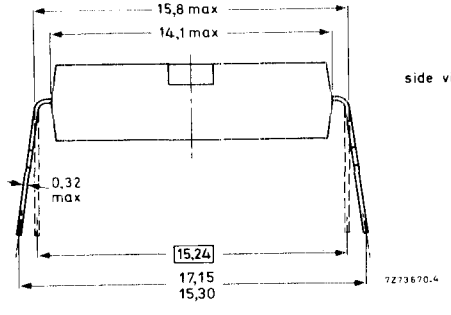


Fig.10 Oscillator/clock configurations

24-LEAD DUAL IN-LINE; PLASTIC (SOT-101A)





M81–1214/11

⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

(3) Index may be horizontal as shown, or vertical.

Dimensions in mm

SOLDERING

see next page

DEVELOPMENT SAMPLE DATA

SOLDERING

1. **By hand**

   Apply the soldering iron below the seating plane (or not more than 2 mm above it).
   If its temperature is below 300 °C it must not be in contact for more than 10 seconds; if between 300 °C and 400 °C, for not more than 5 seconds.

2. **By dip or wave**

   The maximum permissible temperature of the solder is 260 °C; this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.
   The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

3. **Repairing soldered joints**

   The same precautions and limits apply as in (1) above.