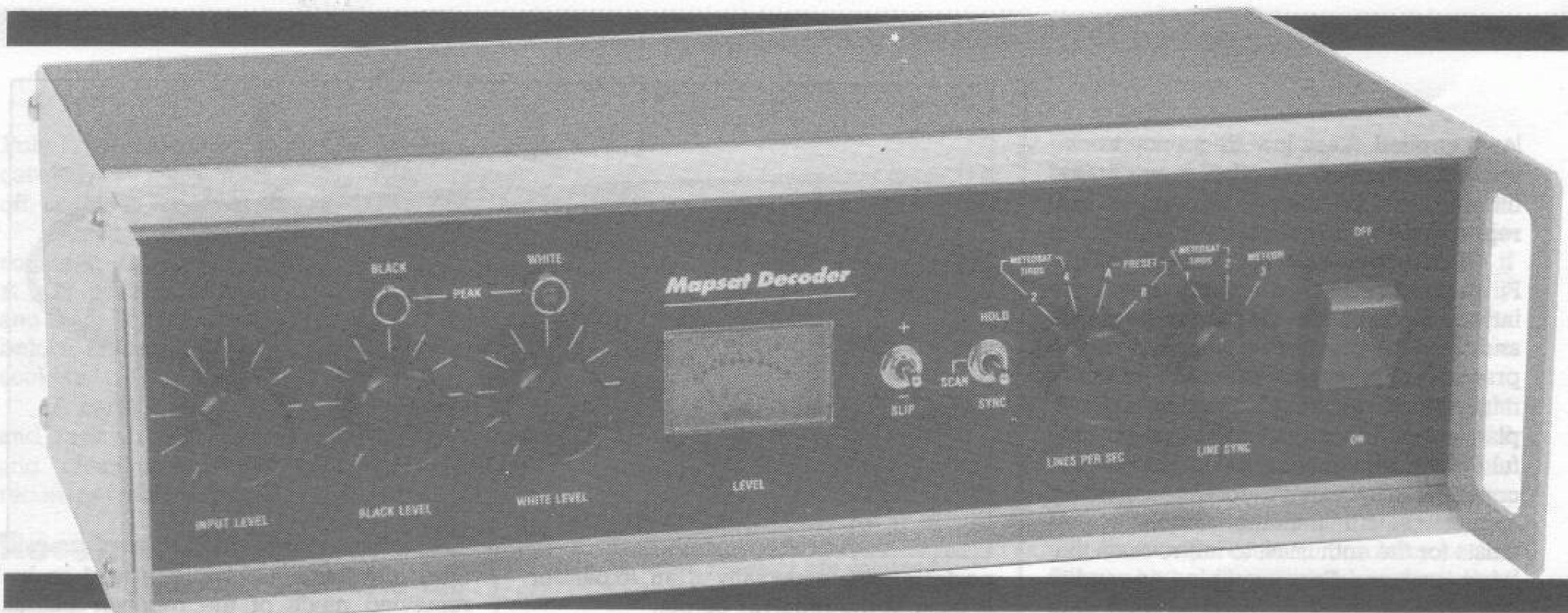
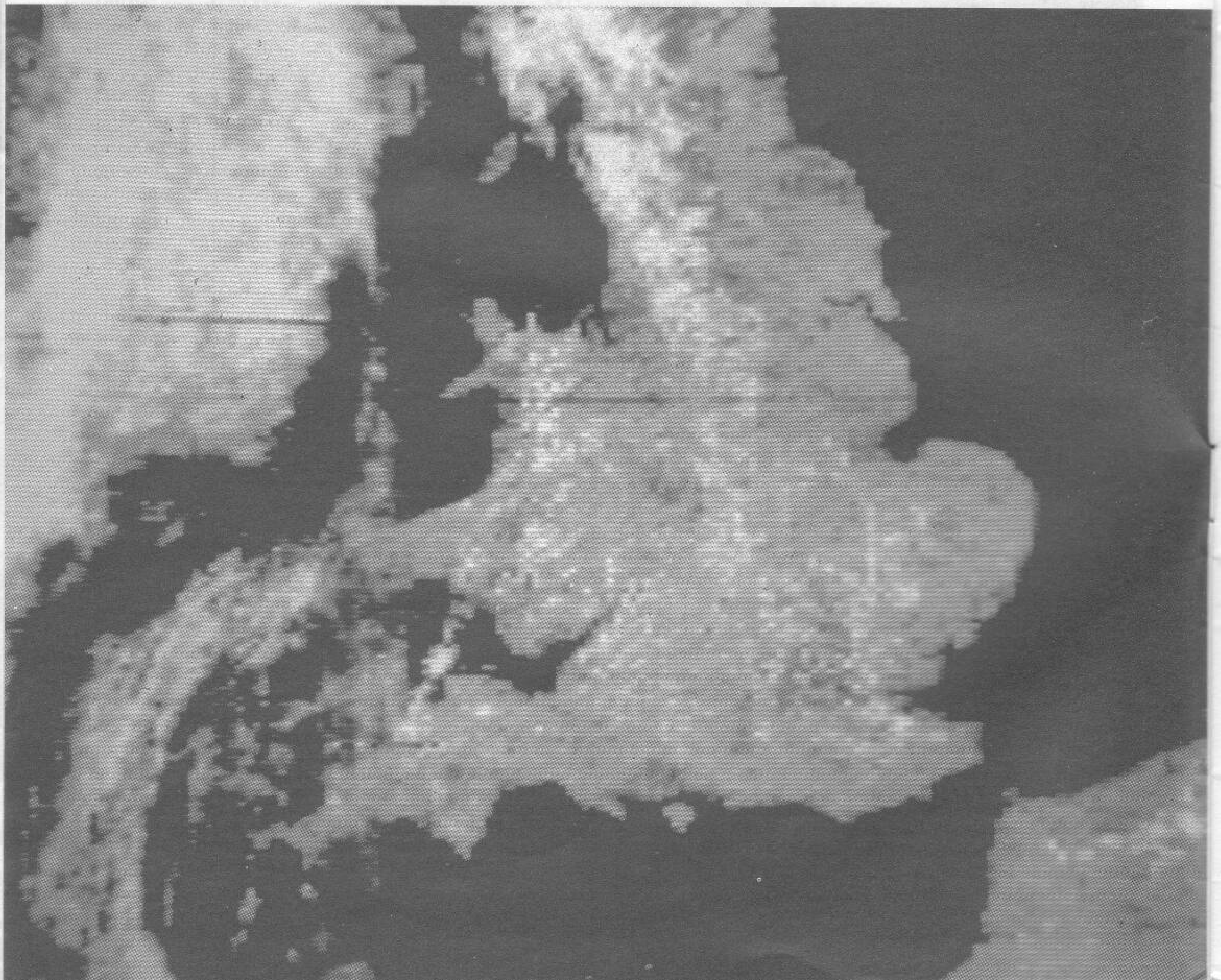


- ★ ***Full 8-bit Digital Output***
- ★ ***Picture Slip Control***
- ★ ***Black and White Level Controls***
- ★ ***Input Level Meter***
- ★ ***Peak White and Black Indicators***
- ★ ***Optional Line Sync Card***
- ★ ***Sync Timing for TIROS Satellites Provided***
- ★ ***Programmable Sync Cards for Other Satellites***
- ★ ***Built-in Power Unit (Also Supplies Receiver)***



SATELLITE DECODER

by Robert Kirsch Part 2

The Decoder

This article describes the Decoder needed to demodulate the APT (Automatic Picture Transmission) signals transmitted from most of the orbiting and geostationary weather satellites. These signals can be received using the Receiver described in Part 1 of this series.

The Decoder accepts audio signals either from tape or directly from the receiver and converts them into an 8-bit digital format with necessary synchronising pulses for connection to a suitable computer or frame store for display on a television or monitor. Controls are provided to enable the contrast of the picture to be adjusted and various types of synchronisation may be selected to suit different satellites. Power for the decoder comes from an internal power unit which will also supply the receiver.

The APT Format

Pictures transmitted by most VHF American and Russian orbiting weather satellites, as well as WEFAX transmissions from the GOES series satellites (e.g. ESA METEOSAT 2), use the APT format. The radio frequency carrier is frequency modulated by a 2.4kHz subcarrier whose amplitude is modulated by the picture information and synchronising signals. Figure 1 shows the subcarrier envelope for a typical line of APT information.

Peak white, it will be noted, corresponds to maximum subcarrier level, and black to the minimum. Picture lines are transmitted either 2 or 4 times a second, each line having 600 cycles of subcarrier, thus the maximum horizontal definition is 600 pixels. The TIROS satellites send alternate lines of infra-red and visible information (when viewing the Earth in daylight) each line being preceded by synchronising pulses. Channel 1 (visible) sends 7 pulses at 1040 pulses per second and channel 2 (infra-red) sends 7 pulses at 832 pulses per second. Meteosat sends 7 pulses at 840 pulses per second at the start of every line, as well as a 300 pulses per second start and a 450 pulses per second stop signal for frame synchronisation.

Decoder with the Receiver

The Russian Meteor satellites send approximately 2 lines per second with a synchronising tone of 300Hz for every line. The decoder described in this article produces line synchronising pulses by dividing the 2.4kHz subcarrier digitally, using a programmable divider to obtain the correct periods for various types of satellites. These pulses may be manually adjusted to correctly position the picture on the screen. (When using the optional sync tone decoder card this is achieved automatically.)

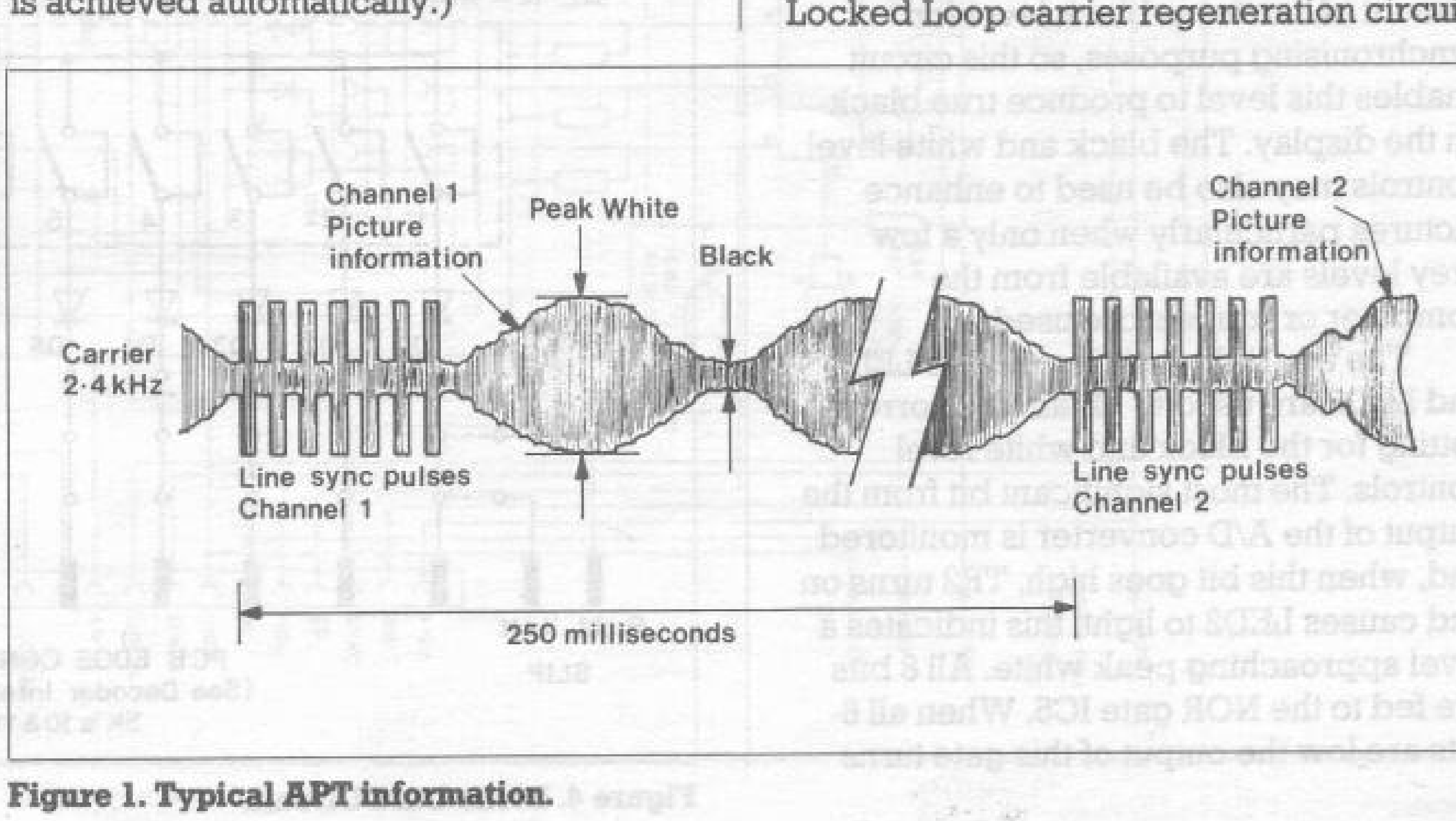


Figure 1. Typical APT information.

Circuit Description

Figure 2 shows a block diagram of the decoder, synchronising unit and power supply. Figure 3 shows the circuit diagram for the main circuit board. Live or recorded signals, selected by the receiver, enter via the 6-pin DIN socket and are first fed to a master level control. The signal at this point splits into three paths; the first goes to the A/D converter, the second to the Level Meter and AM detector circuit, and the third to the Phase Locked Loop carrier regeneration circuit.

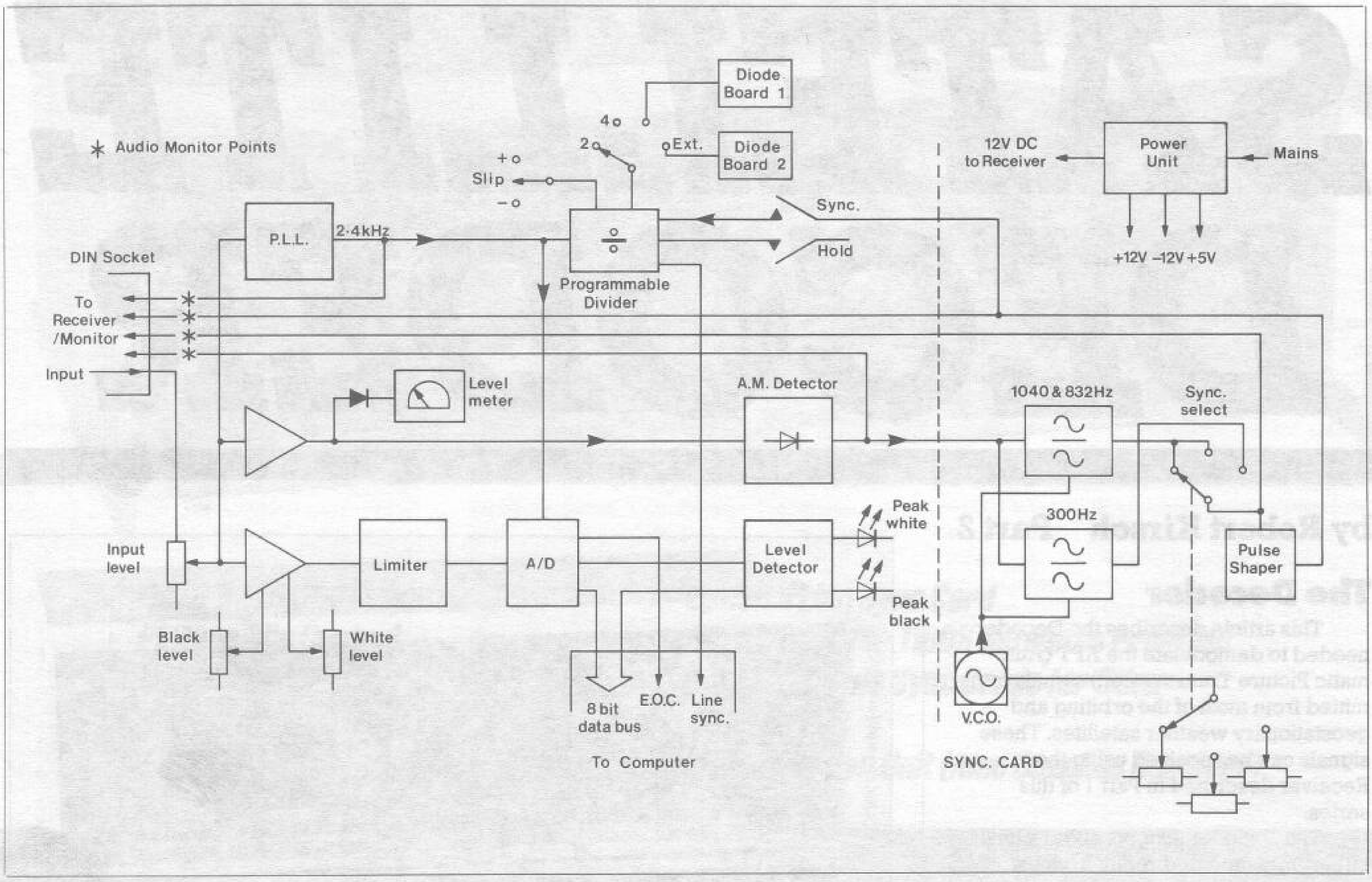


Figure 2. Decoder Block Schematic.

The conversion from the analogue subcarrier level to a digital code is accomplished by IC2, an 8-bit A/D converter. This device requires two inputs, one is the analogue information, and the other is a 'start conversion pulse'. The analogue input range of IC2 is from 0 to 2.5 volts to give codes from black to peak white. It is therefore important to adjust the level of the incoming signal in order to obtain correct contrast on the displayed picture. This function is provided by the op-amp IC1a. The gain of this device is adjusted by RV5 in the feedback circuit, this sets the white level. The output from IC1a is about ± 2.5 volts but only the positive half cycle is fed to the A/D converter. RV4 sets the DC reference of the op-amp, and this offset is used to adjust the black level of the picture. Note, there is always a small amount of carrier at black level for synchronising purposes, so this circuit enables this level to produce true black on the display. The black and white level controls may also be used to enhance pictures particularly when only a few grey levels are available from the computer or frame store used.

The two light emitting diodes LED1 and LED2 are used to obtain the correct setting for the black and white level controls. The most significant bit from the output of the A/D converter is monitored and, when this bit goes high, TR2 turns on and causes LED2 to light, this indicates a level approaching peak white. All 8 bits are fed to the NOR gate IC5. When all 8-bits are low the output of this gate turns TR1 on, causing LED1 to light and indicate black level.

The second op-amp, IC1b, is fed with the incoming signal via the input level control. The output from IC1b is rectified by D3 and D4 to drive the level meter which should read full scale on a peak white signal. The AM detector formed by D1 and D2 is also fed from the output of IC1b and this audio signal is fed to the sync tone decoder card.

The phase locked loop, IC3, is fed with the incoming modulated signal and locks to the 2.4kHz subcarrier. The clean square wave output produced is used to generate the 'start conversion' pulse for the A/D converter and it is also fed to the programmable divider to produce line synchronising pulses.

The three counters IC6, 7 and 8 form the programmable divider whose division ratio is set by the data on pins 3, 4, 5 and 6 of each IC. The rotary switch S2 selects one of two preset ratios (1200 for 2 lines per second and 600 for 4 lines per second) and also two ratios that may be set by programming the optional diode cards, the circuit of which is shown in Figure 4. The SLIP control, S3, temporarily raises or lowers the division ratio to enable the picture to be moved in relation to the line sync pulse thus shifting the display left or right in relation to the television screen. The phase locked loop will produce an output even when no input is present, and therefore line sync pulses will also occur. For this reason the HOLD switch is provided to stop the

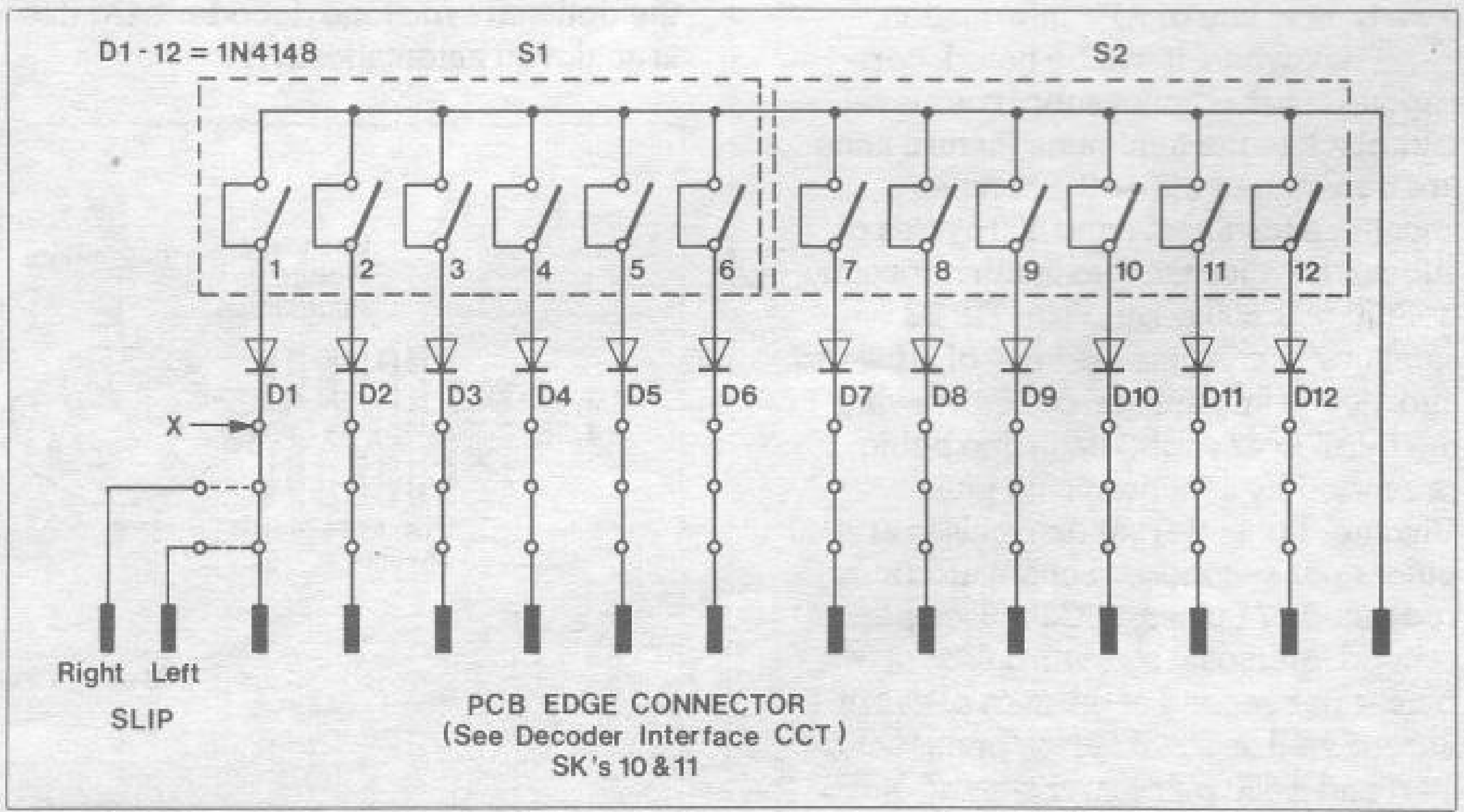


Figure 4. Diode Card Circuit.

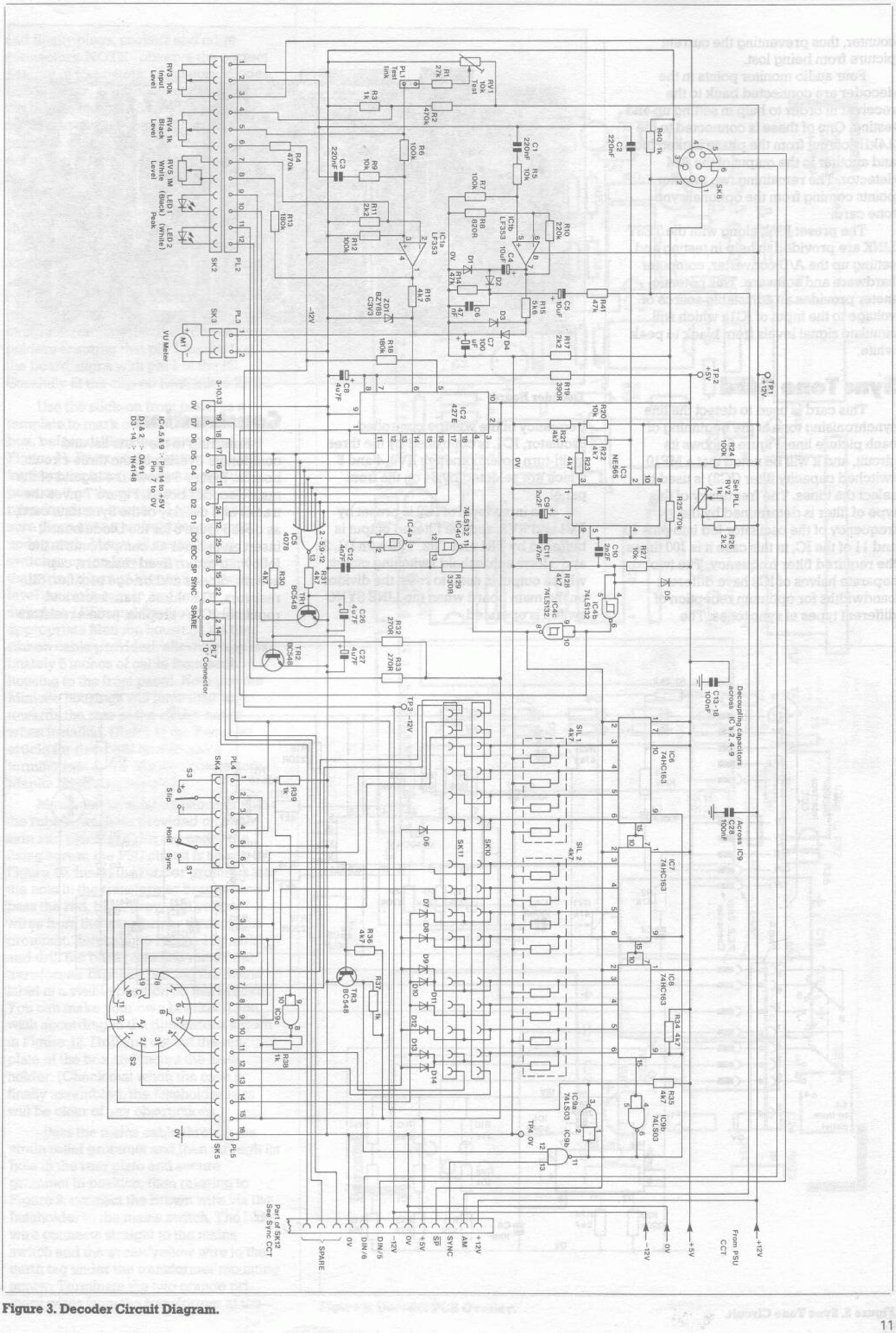
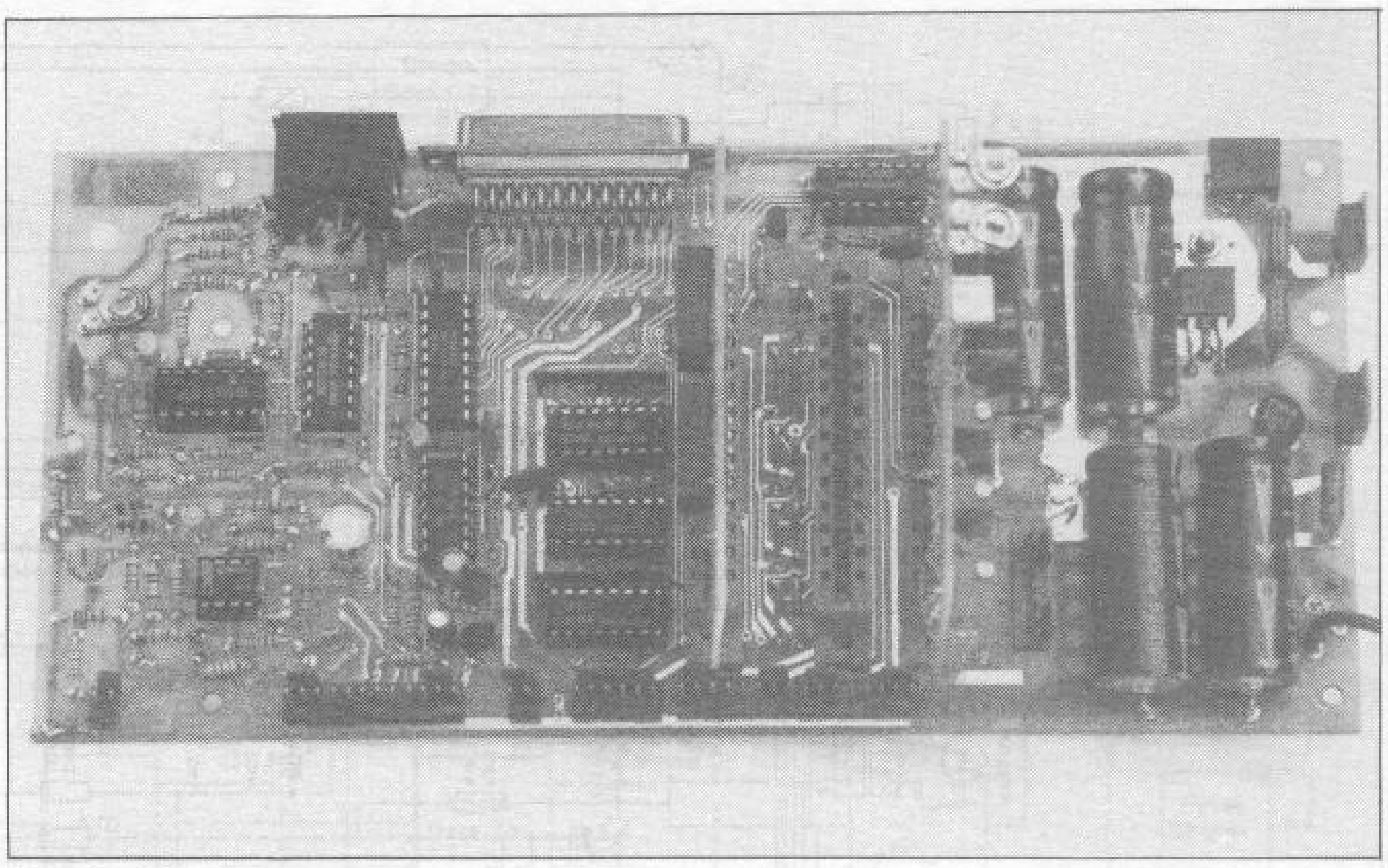


Figure 3. Decoder Circuit Diagram.

counter, thus preventing the current picture from being lost.

Four audio monitor points in the decoder are connected back to the receiver in order to help in setting up and testing. One of these is connected to the 2.4kHz output from the phase locked loop and another to the output of the AM detector. The remaining two monitor points coming from the optional sync tone card.

The preset RV1, along with the TEST LINK are provided to help in testing and setting up the A/D converter, computer hardware and software. This potentiometer provides an adjustable source of voltage to the input of IC1a which will simulate signal levels from black to peak white.



Decoder Board

Sync Tone Card

This card is used to detect the line synchronising tone at the beginning of each picture line. Figure 5 shows its circuit, and it will be noted that a MF10 switched capacity filter (IC2) is used to select the tones. The frequency of this type of filter is determined by the frequency of the oscillator fed into pins 10 and 11 of the IC, in this case it is 100 times the required filter frequency. The two separate halves of IC2 have different bandwidths for optimum reception of different types of sync tones. The frequency of the voltage controlled oscillator, IC1, is controlled by the three multi-turn potentiometers RV3, 4 and 5 which are selected by S4 on the front panel.

The input level of IC2 is preset by RV1 and RV2, and the filtered output is buffered by TR1 and TR2. TR3 with D1, 2 and 3 form a threshold switching circuit whose output is used to reset the divider on the main board when the LINE SYNC switch is operated.

Construction

Referring to the Parts list and component overlay on the three circuit boards, Figure 6 shows the legend of the main decoder board, Figure 7 gives the tracks and overlay of the Sync tone card, as does Figure 8 for the Diode board; insert and solder all components in the following order: fixed resistors, capacitors, diodes and bridge rectifier, SIL resistors, IC holders, transistors and regulator IC's; veropins, preset resistors

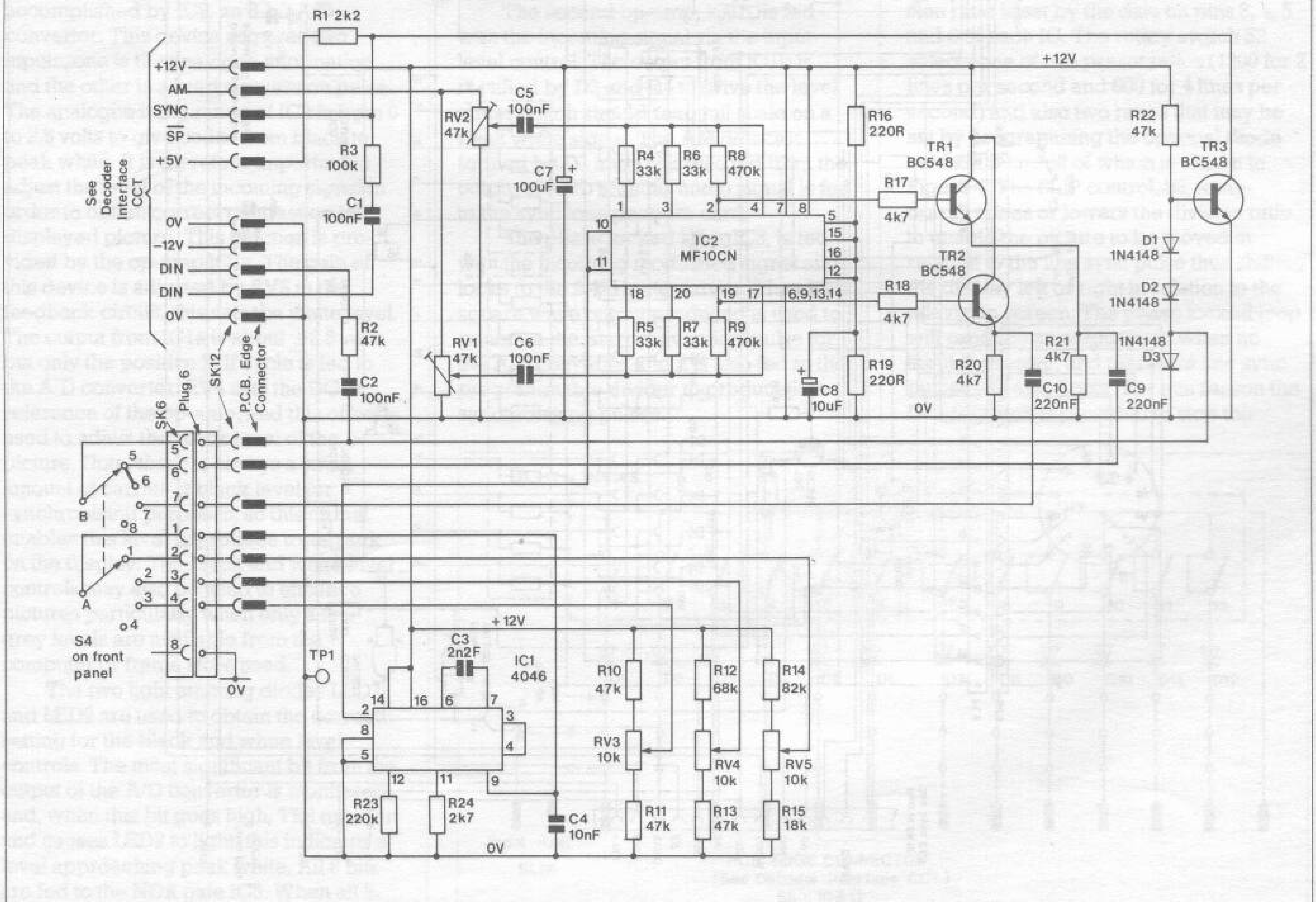


Figure 5. Sync Tone Circuit.

and finally plugs, sockets and edge connectors. **NOTE** - observe the correct polarity of transistors, regulators, diodes, LED's, meter, electrolytic capacitors and the bridge rectifier. The white dot marked at one end of the SIL resistor package should correspond to the white dot on the board overlay. The tags of the Minicon plugs should be to the rear of the circuit board. The white rings on the overlays indicate where the boards should be soldered on *both* sides; in addition TR1 on the sync card should be soldered on both sides also.

Insert the keys into the edge connectors, referring to the wiring diagram Figure 9. Carefully insert all integrated circuits into their correct holders ensuring that pin 1 marked on the board aligns with pin 1 of the IC. Carefully fit the clip-on heatsink to REG2.

Use the stick-on front panel as a template to mark out the front plate of the box, before drilling and cutting out, see Figure 11. Remove the protective backing from the front panel and carefully position it on the prepared front plate, pressing down evenly all over, making sure there are no air bubbles trapped underneath. Mount all controls and switches on the front panel. Referring to the wiring diagram Figure 9, connect all level controls, toggle and rotary switches, LED's and the meter to their appropriate Minicon housings via the ribbon cable provided, allowing approximately 5 inches of cable from each housing to the front panel. Note that the Minicon housings will have their lugs towards the rear of the circuit board when installed. (Refer to the Receiver article for details of how to make terminations to the Minicon connectors, Maplin Magazine Issue 18.)

Mount the toroidal transformer with the rubber washers provided on either side and place a solder tag under the fixing screw, the PSU circuit is shown in Figure 10. Insert the rubber grommet into the hole in the transformer bracket and pass the red, blue, grey, and yellow wires from the transformer through the grommet. Referring to Figure 11, mark and drill the base plate and mount the transformer bracket, placing the mains label in a visible position on this bracket. You can make your own bracket if you wish according to the dimensions shown in Figure 12. Drill and cut out the rear plate of the box and mount the fuseholder. (Check that when the case is finally assembled, the fuseholder tags will be clear of any obstructions.)

Pass the mains cable through the strain relief grommet and then through its hole in the rear plate and secure grommet in position, then refering to Figure 9, connect the brown wire via the fuseholder to the mains switch. The blue wire connects straight to the mains switch and the green/yellow wire to the earth tag under the transformer mounting screw. Terminate the two orange primary wires from the transformer at the

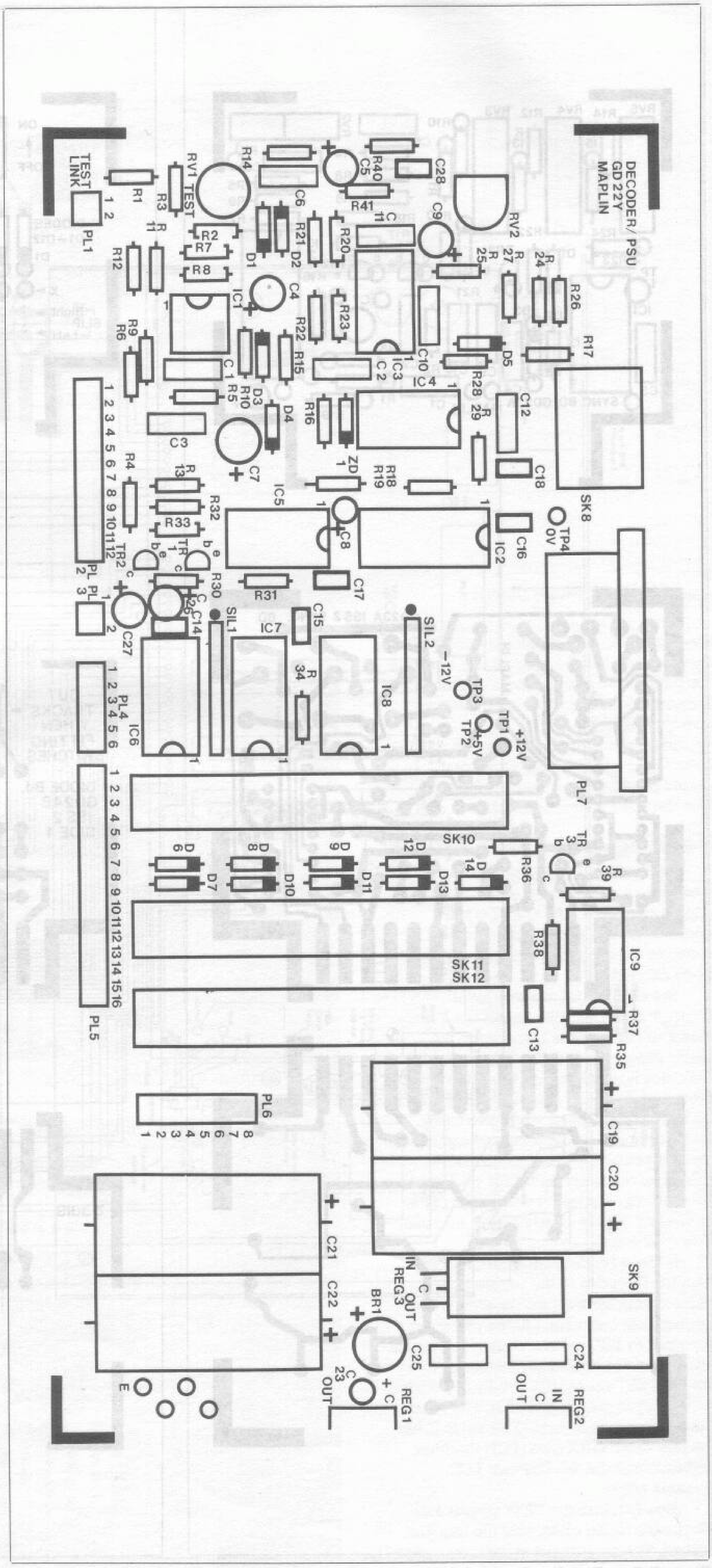


Figure 6. Decoder PCB Overlay.

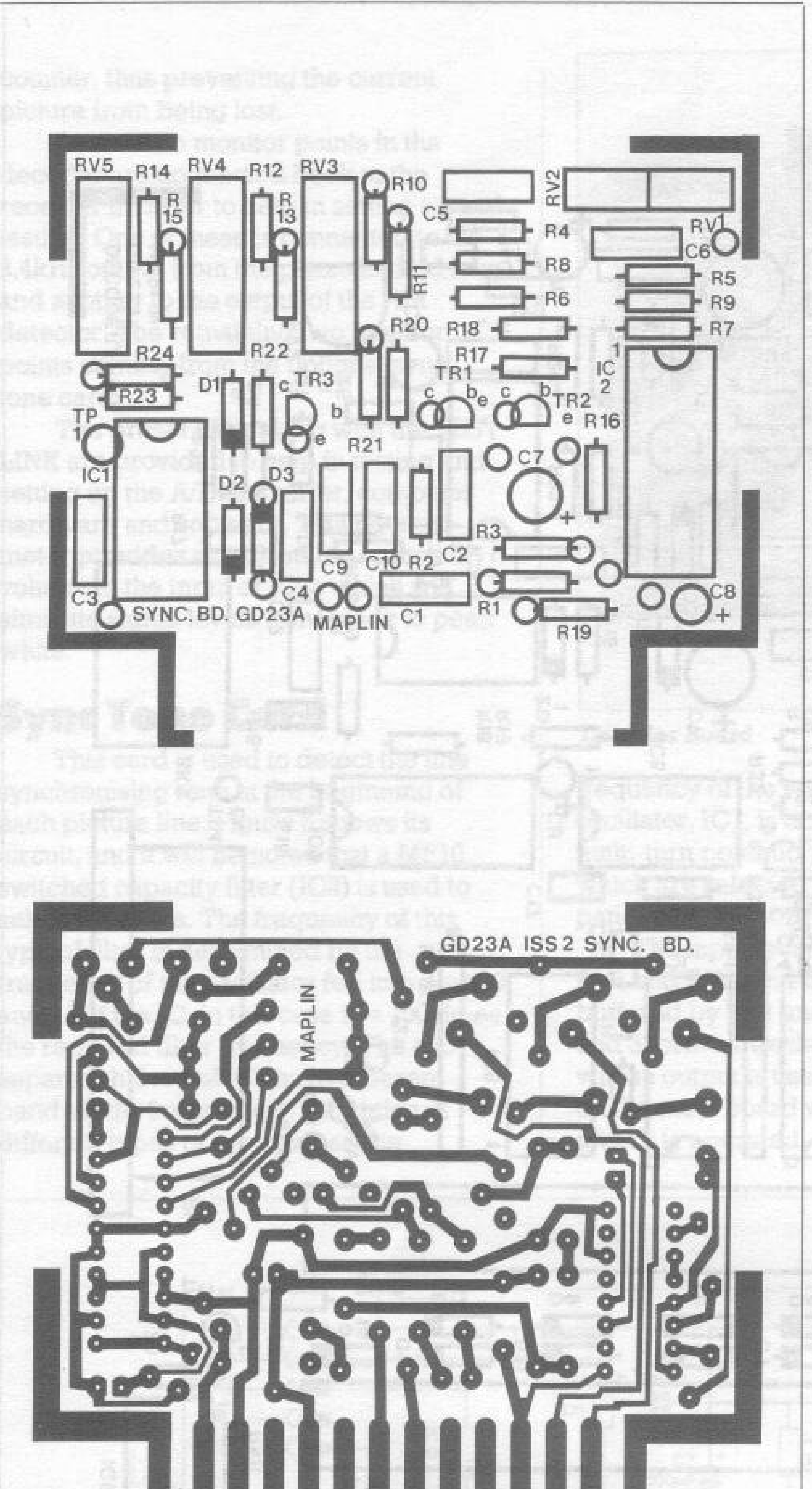


Figure 7. Sync Tone Tracks and Overlay.

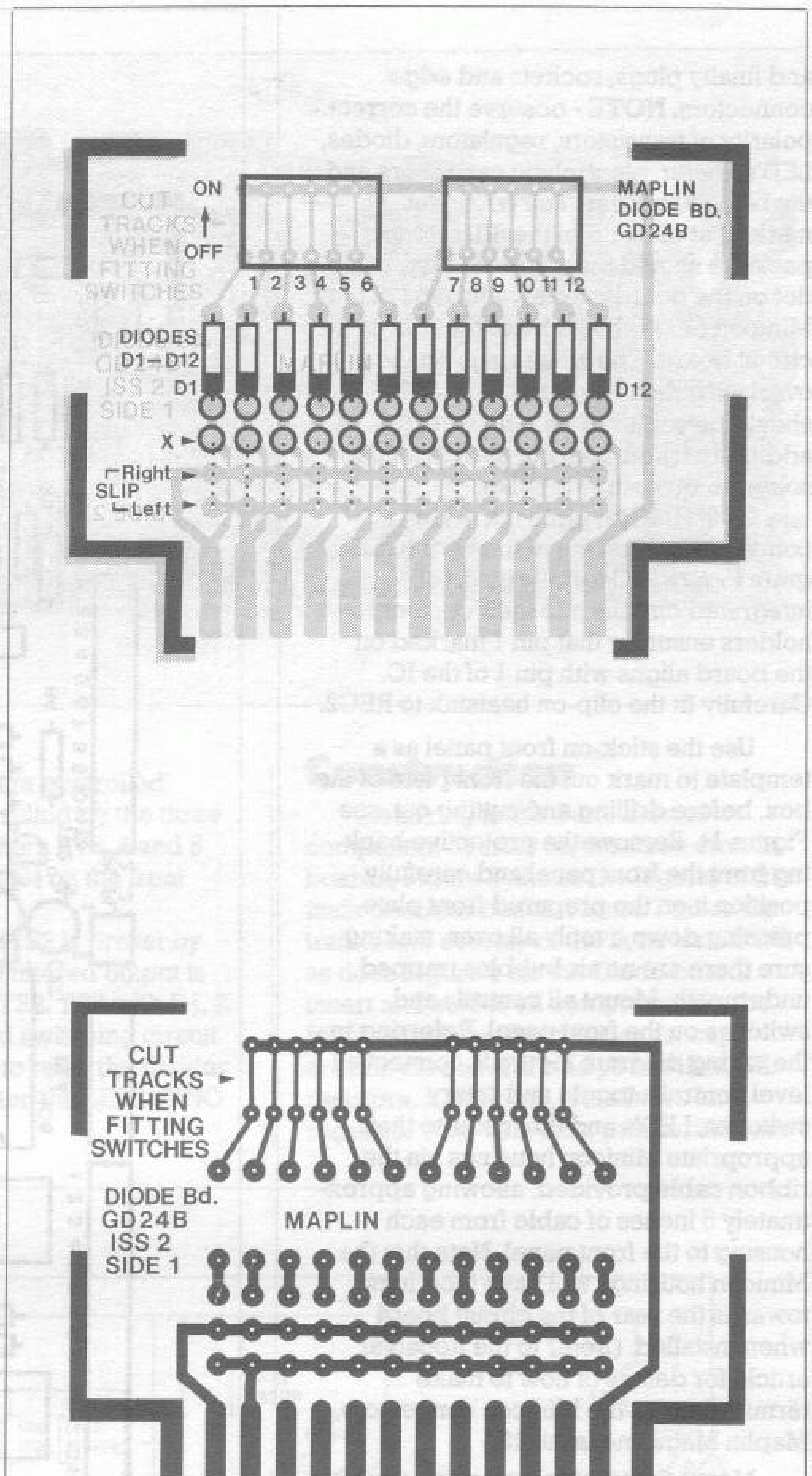


Figure 8. Diode Board Tracks and Overlay.

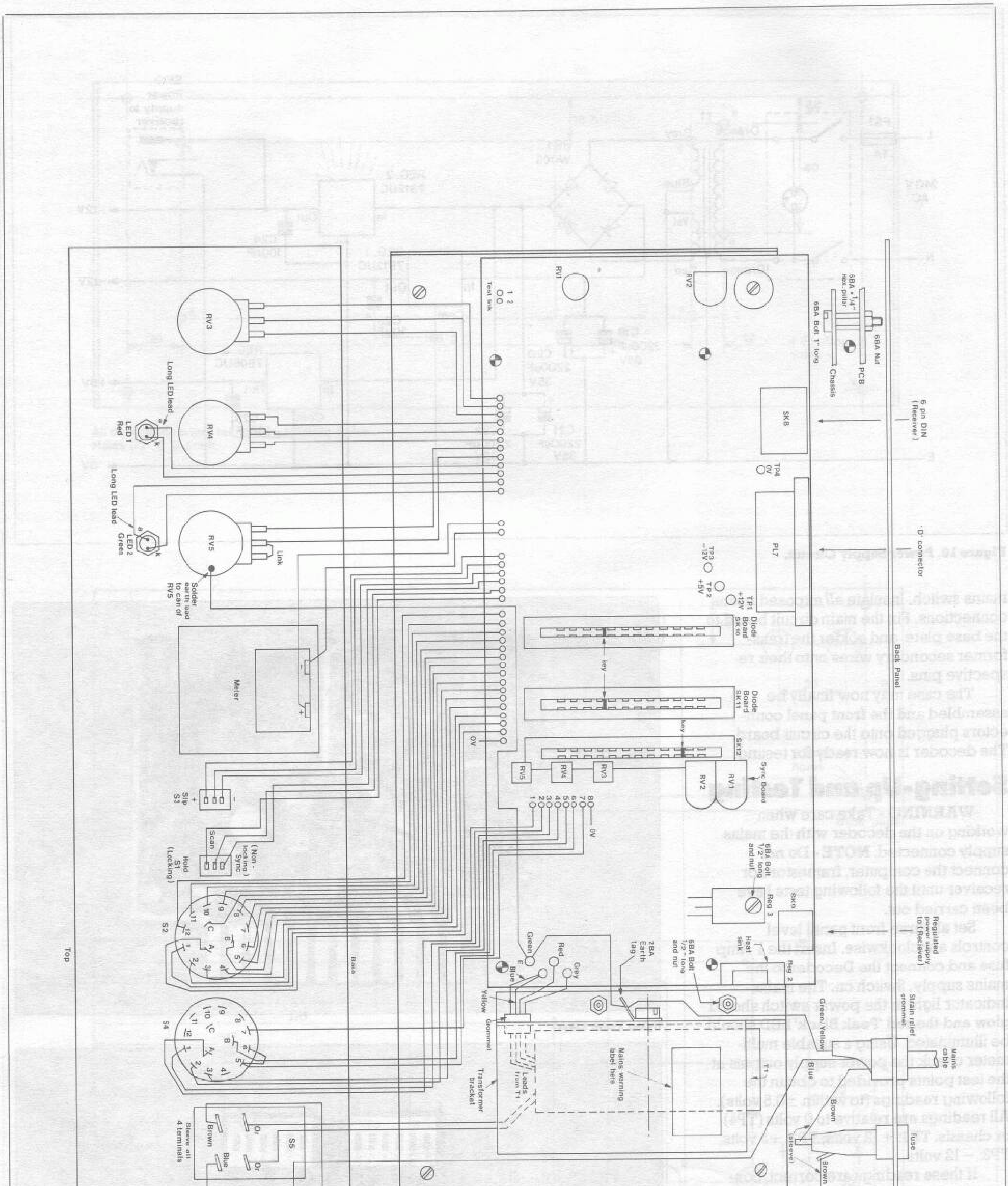


Figure 9. Wiring Diagram.

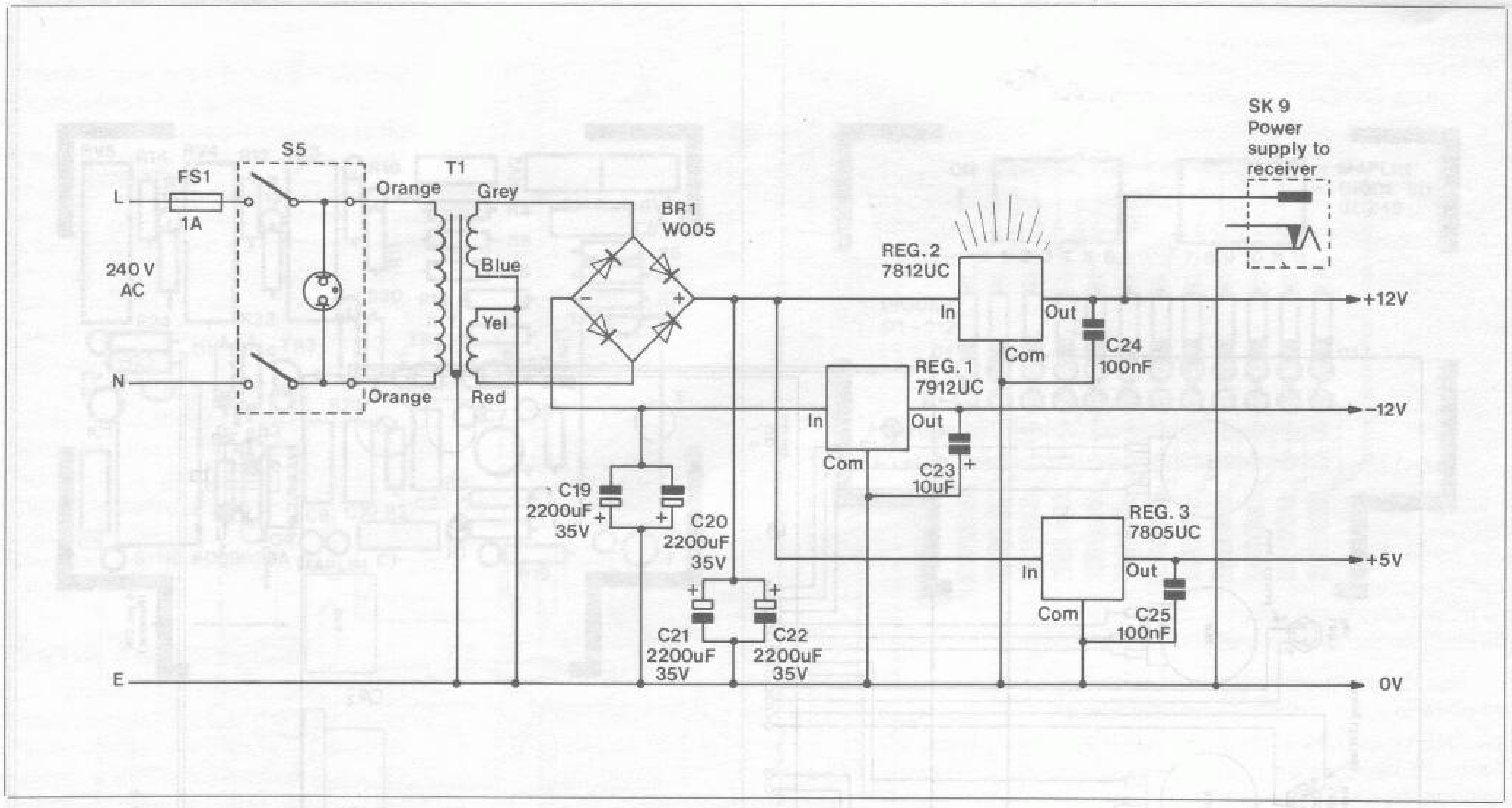


Figure 10. Power Supply Circuit.

mains switch. Insulate *all* exposed mains connections. Fix the main circuit board to the base plate, and solder the transformer secondary wires onto their respective pins.

The case may now finally be assembled and the front panel connectors plugged onto the circuit board. The decoder is now ready for testing.

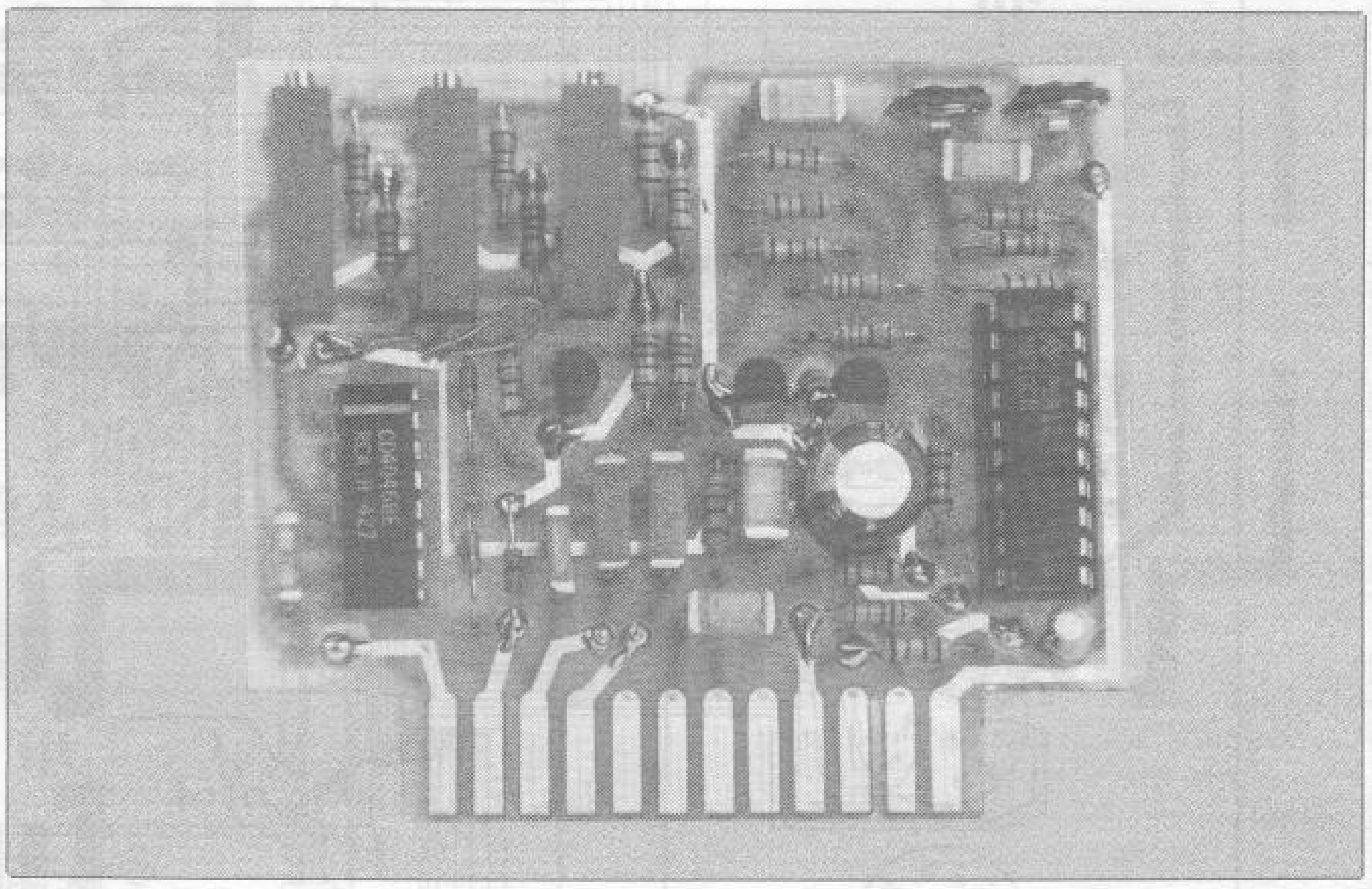
Setting-Up and Testing

WARNING - Take care when working on the decoder with the mains supply connected. **NOTE** - Do *not* connect the computer, framestore or receiver until the following tests have been carried out.

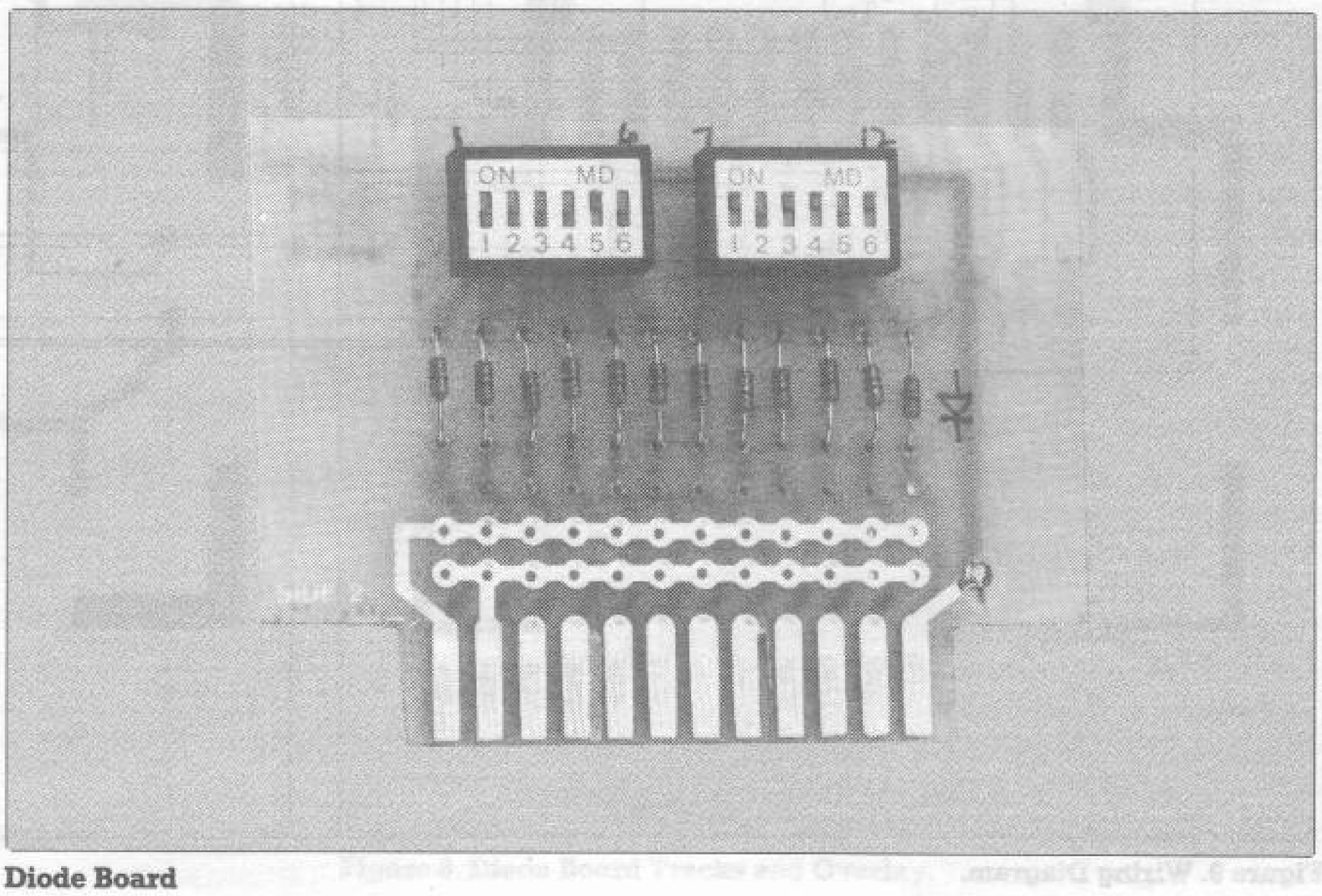
Set all three front panel level controls anticlockwise. Insert the 1 Amp fuse and connect the Decoder to the mains supply. Switch on. The mains indicator light in the power switch should glow and the red 'Peak Black' LED should be illuminated. Using a suitable multimeter check the power supply outputs at the test points provided to obtain the following readings (to within ±0.5 volts). All readings are relative to 0 volts (TP4) or chassis. TP1: +12 volts, TP2: +5 volts, TP3: −12 volts.

If these readings are correct, connect the Decoder to the parallel I/O port of the computer/framestore and run the appropriate software. (When using the Amstrad or BBC software provided in this article, set the horizontal resolution to 4.) Set the TEST preset (RV1) fully clockwise and the sync switch to SCAN. The lines per second switch should be set to 2. Join the two TEST LINK pins (PL1) together and note that the 'Black Peak' LED remains alight.

Slowly rotate the TEST preset anticlockwise whilst observing the monitor screen. The brightness of the scan lines moving up the screen should be seen to



Sync Tone Card



Diode Board

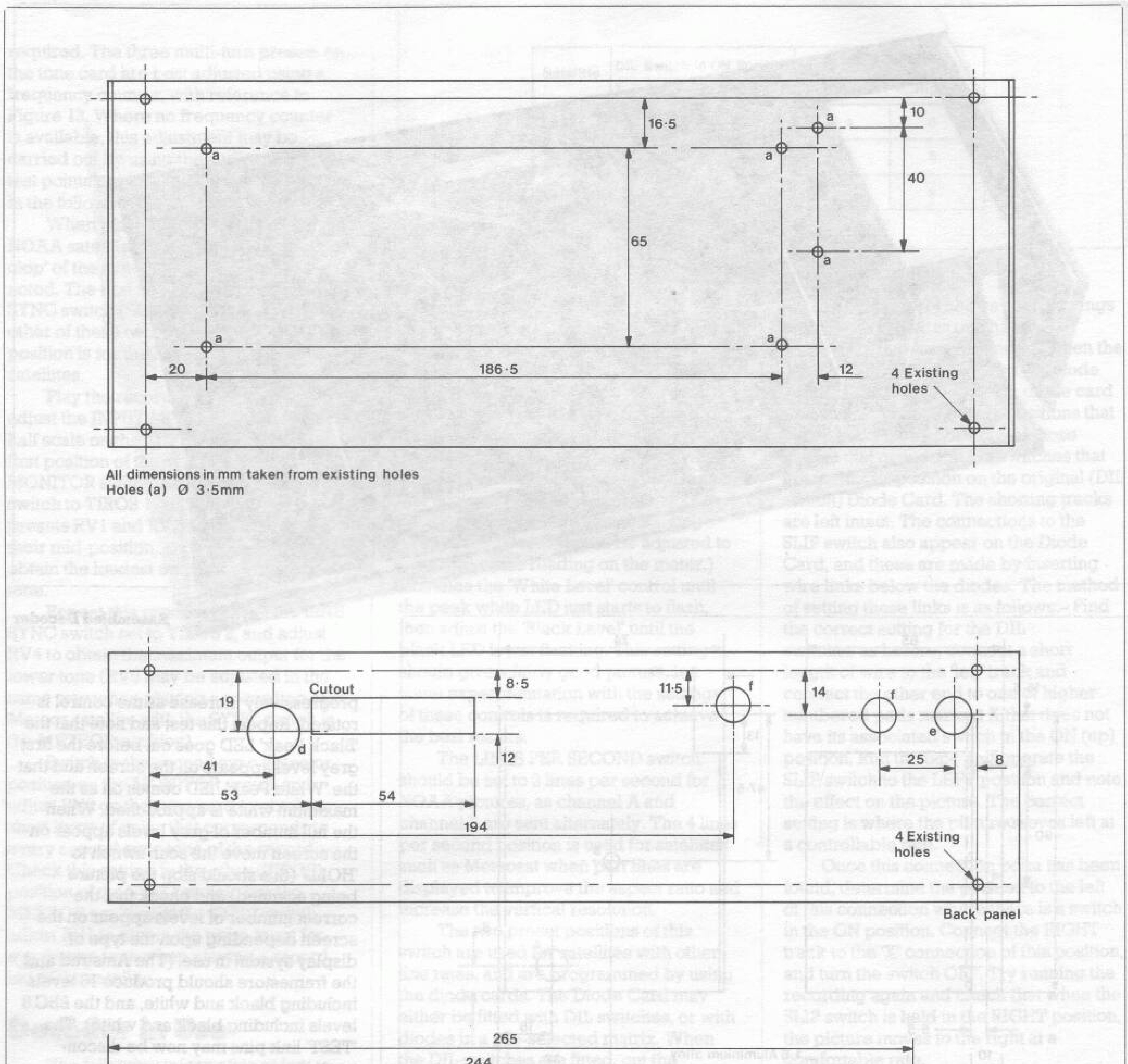
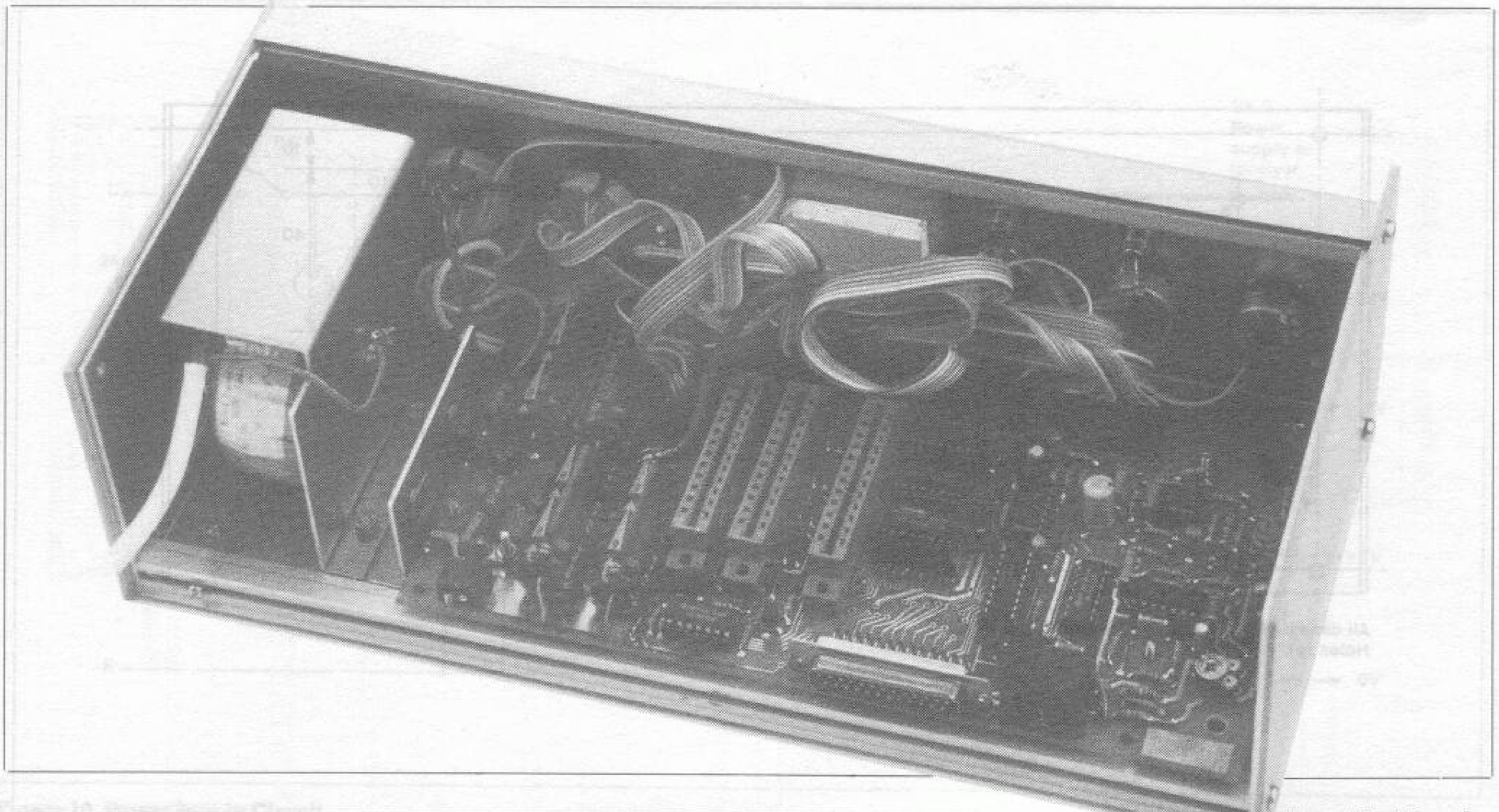


Figure 11. Case Cut-out Details.



Assembled Decoder

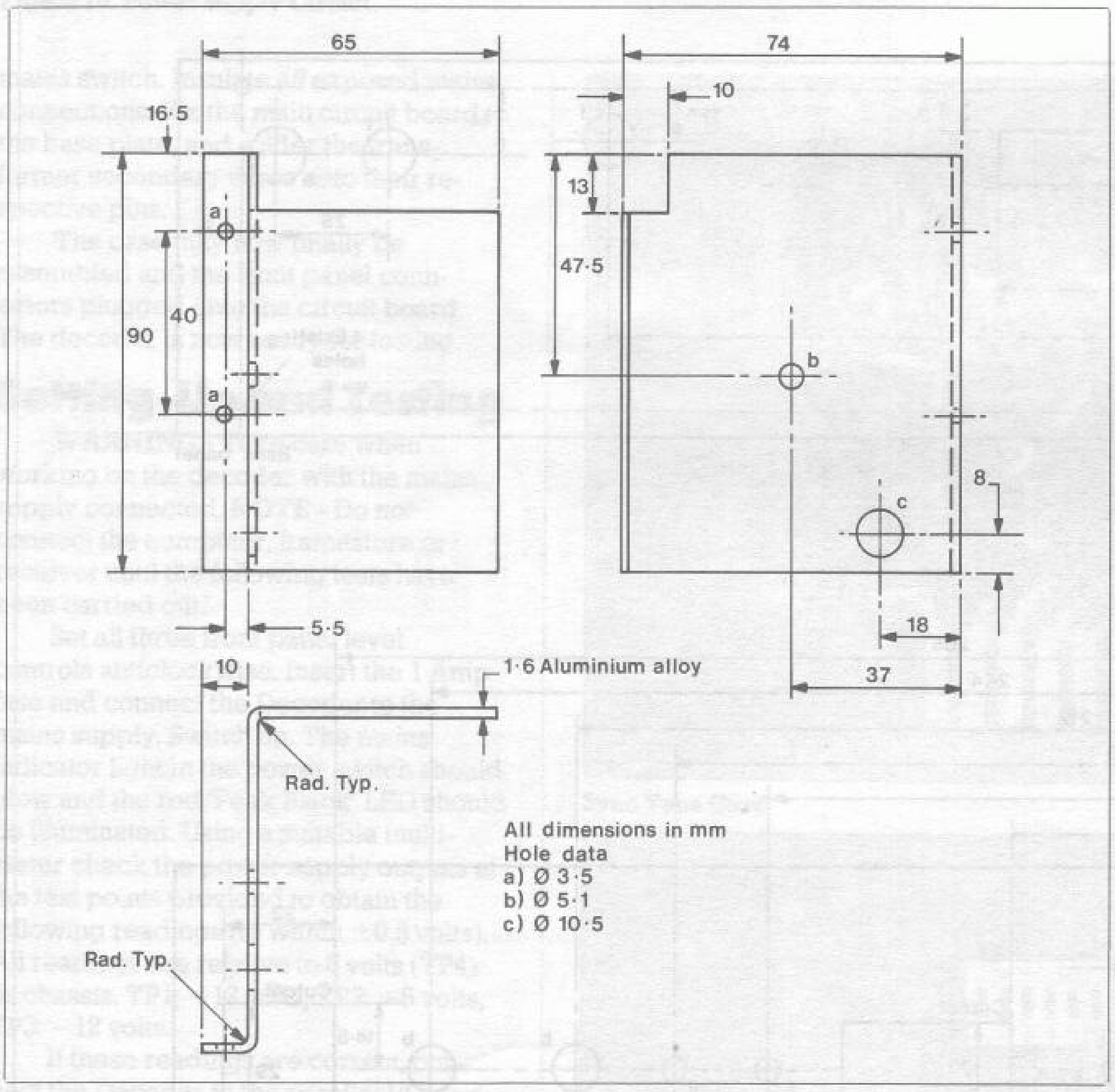


Figure 12. Transformer Bracket.

Sync Tone Switch Position	Frequency of Tone	Frequency at TP1 of Sync Tone Card
TIROS 1 (Channel A)	1040Hz	104 kHz
TIROS 2 (Channel B)	832Hz	83·2kHz
METEOR	300Hz	30kHz

Figure 13. Sync Card Frequency Settings.

progressively increase as the control is rotated. Repeat this test and note that the 'Black Peak' LED goes out before the first grey level appears on the screen and that the 'White Peak' LED comes on as the maximum white is approached. When the full number of grey levels appear on the screen move the scan switch to 'HOLD' (this should stop the picture being scanned) and check that the correct number of levels appear on the screen depending upon the type of display system in use. (The Amstrad and the framestore should produce 16 levels including black and white, and the BBC 8 levels including black and white). The 'TEST' link pins may now be disconnected.

The following tests should be carried out by using a good quality recording of the NOAA 6 or NOAA 9 satellites. Connect the Decoder to the Receiver via the 6-way audio DIN lead and the power lead. Connect the tape recorder to the Receiver, referring to the previous article (Issue 18). Play the recording of the satellite. Select TAPE OUT on the MONITOR switch of the Receiver and adjust the VOLUME to a comfortable level. Set the Decoder INPUT LEVEL control to minimum. Switch between TAPE OUT and PLL on the MONITOR switch, and adjust the preset RV2 on the Decoder board until the tone from the PLL is the same as that of the satellite's subcarrier.

To check this setting, the INPUT LEVEL may now be increased and the 'Black Level' LED should now flash or go out. Check that the LEVEL meter responds as the INPUT LEVEL control is increased.

The basic Decoder is now ready for use but if the sync tone card has been installed the following setting-up is required. The three multi-turn presets on the tone card are best adjusted using a frequency counter, with reference to Figure 13. Where no frequency counter is available, this adjustment may be carried out by using the audio monitor test points provided in the Receiver unit in the following manner.

When playing a recording of the NOAA satellites, the characteristic 'clip-clop' of the synchronising tones will be noted. The first two positions of the LINE SYNC switch ('TIROS') select one or other of these two tones, the third position is for the Russian Meteor satellites.

Play the recording as before and adjust the INPUT LEVEL to give about half scale on the LEVEL meter. Select the first position of the sync detector on the MONITOR switch. Switch the LINE SYNC switch to TIROS 1, and set the two presets RV1 and RV2 on the sync card to their mid-position, and adjust RV3 to obtain the loudest output for the *higher* tone.

Repeat this procedure with the LINE SYNC switch set to TIROS 2, and adjust RV4 to obtain the maximum output for the *lower* tone (RV5 may be adjusted in the same way when playing a recording of a Meteor satellite with the SYNC switch in the METEOR position).

Switch to the second sync detector position on the MONITOR switch and adjust RV2 on the sync card to obtain a short burst of noise that corresponds to every second sync tone of the recording. Check this setting in the other (TIROS) position of the SYNC switch. For the METEOR position of the SYNC switch, adjust RV1 to obtain the noise burst for every sync tone when playing a recording of the satellite.

Decoder in Use

The following information refers to the use of the decoder with the BBC B and Amstrad computers. (Information for using the Frame Store will be published later).

Program 1 is for the BBC model B, Program 2 is the machine code created by the GENA 3 assembly program from Amsoft. From Program 2 you can create your object file which can then be loaded by Program 3. When loaded and run, these will ask for the Horizontal Resolution to be entered; this value determines not only the definition of the displayed picture, but also the proportion of the total picture width displayed across the screen. The first time a recording is run, select full width (4), and then any interesting parts may be re-run with a lower setting to obtain greater detail. The SHIFT switch may be used to move the picture to the desired position at the beginning of the run, and if required, the full scan may be re-started by holding the space bar. (The sync when set is not lost until the tape is stopped or the signal fails.) Synchronisation to the start of a line is provided by the Sync Tone Card. The

Satellite	DIL Switch in ON Position												Slip Switch Connections	
	1	2	3	4	5	6	7	8	9	10	11	12	Left	Right
# 1	√		√	√		√						√	9	8
# 2	√		√	√					√	√	√		8	6
# 3	√		√	√		√							9	8

Figure 14. Settings for Russian Satellites.

LINE SYNC switch selects the type of satellite and channel to be synchronised. With the recording running and the appropriate position of the LINE SYNC switch set, synchronisation is achieved by a short operation of the non-locking SYNC toggle switch.

The INPUT LEVEL control should be set to give an average reading of about half scale on the LEVEL meter. (Note that if a known peak white signal is being received, the level should be adjusted to give a full scale reading on the meter.) Advance the 'White Level' control until the peak white LED just starts to flash, then adjust the 'Black Level' until the black LED is just flashing. This setting should give a fairly good picture, but some experimentation with the settings of these controls is required to achieve the best results.

The LINES PER SECOND switch should be set to 2 lines per second for NOAA pictures, as channel A and channel B are sent alternately. The 4 lines per second position is used for satellites such as Meteosat when part lines are displayed to improve the aspect ratio and increase the vertical resolution.

The two preset positions of this switch are used for satellites with other line rates, and are programmed by using the diode cards. The Diode Card may either be fitted with DIL switches, or with diodes in a pre-selected matrix. When the DIL switches are fitted, cut the shorting tracks under the switches, and fit all diodes. The correct setting for a satellite is found by switching the LINES PER SECOND switch to the A position, inserting a diode card, with DIL switches installed, in position (nearest to the sync card) and trying different settings of the switches until a synchronised picture is obtained. Figure 14 shows some settings for Russian satellites that have been found to synchronise correctly. When the setting has been determined, the code may be 'copied' onto a blank diode card by inserting diodes *only* in positions that correspond to the positions of those diodes that connect to the switches that are in the ON position on the original (DIL switch) Diode Card. The shorting tracks are left intact. The connections to the SLIP switch also appear on the Diode Card, and these are made by inserting wire links below the diodes. The method of setting these links is as follows:– Find the correct setting for the DIL switches as before, connect a short length of wire to the 'left' track and connect the other end to one of higher numbered pads marked X that does not have its associated switch in the ON (up) position. Run the tape and operate the SLIP switch to the LEFT position and note the effect on the picture. The correct setting is where the picture moves left at a controllable rate.

Once this connection point has been found, determine the position to the left of this connection where there is a switch in the ON position. Connect the RIGHT track to the 'X' connection of this position, and turn the switch OFF. Try running the recording again and check that when the SLIP switch is held in the RIGHT position, the picture moves to the right at a comfortable rate.

When the correct positions for the two connections have been found, permanent wire links may be fitted.

The picture scanning may be stopped at any time by using the HOLD switch. (This does not lose synchronisation if the incoming signal is uninterrupted.)

DECODER DIODE BOARD PARTS LIST

SEMICONDUCTORS

D1-12	1N4148	12	(QL80B)

MISCELLANEOUS

S1,2	DIL Switch SPST 6-Way	2	(FV44X)
	Diode PCB	1	(GD24B)

A complete kit of all parts is available for this project:
Order As LM09K (Decoder Diode Board Kit)
The following item in the above kit list is also available separately, but is not shown in the 1986 catalogue:
Decoder Diode PCB **Order As GD24B**

Program 1.

```
10 MODE 7
20 CLS:PRINT:PRINT
30 PRINT"INPUT HORIZONTAL RESOLUTION (1-4)";
40 INPUT HRES
50 MODE 2
60 VDU 23;8202;0;0;0
70 PRINT
80 DIM CODE% 500
90 ROWBSE=&70
100 ?ROWBSE=((HIMEM+20479) MOD 256)
110 ?(ROWBSE+1)=((HIMEM+20479) DIV 256)
120 DOTBSE=&72
130 ?DOTBSE=((HIMEM+20479)MOD 256)
140 ?(DOTBSE+1)=((HIMEM+20479)DIV 256)
150 SMPL=&74
160 TEMP=&75
170 RWBSSH=&76
180 FINSCN=&78
190 OVBRT=&7A
200 ?FINSCN=((HIMEM)MOD 256)
210 ?(FINSCN+1)=((HIMEM)DIV 256)
220 PORT=&FE60
230 FOR P=0TO2 STEP 2
240 P%=CODE%
250 [OPT P
260 LDA #&02
270 LDX #&00
280 JSR &FFF4
290 .INIT LDA #&00
300 LDX #&00
310 LDY #&00
320 SEI
330 CLD
340 STA &FE62
350 STA SMPL
360 STA TEMP
370 .WTSYNC
380 LDA PORT
390 AND #64
400 BEQ WTSYNC
410 .FINSYNC
420 LDA PORT
430 AND #64
440 BNE FINSYNC
450 .WASTE BIT PORT
460 BMI WASTE
470 .PING BIT PORT
480 BPL PING
490 INX
500 CPX#01
510 BNE WASTE
520 LDX #&00
530 .WTBUSY
540  BIT PORT
550 BMI WTBUSY
560 .WTSMPL
570 BIT PORT
580 BPL WTSMPL
590 INX
600 .RESH CPX #&02
610 BNE WTBUSY
620 LDA PORT
630 AND #&0F
640 LDX #&00
650 STX TEMP
660 LSR A
670 ROL TEMP
680 ROL TEMP
690 ROL A
700 ROL A
710 ROL A
720 ROL A
730 ROL A
740 ROL A
750 ROL OVBRT
760 ROL A
770 ROL TEMP
780 ROL TEMP
790 ROL A
800 ROL TEMP
810 LSR OVBRT
820 BCC TEST
830 LDA#21
840 STA TEMP
850 .TEST  LDA SMPL
860 LSR A
870 BCC ODD
880 ASL TEMP
890 LDA TEMP
900 ORA (DOTBSE,X)
910 STA (DOTBSE,X)
920 JMP NEWDOT
930 .ODD
940 LDA TEMP
950 STA (DOTBSE,X)
960 .NEWDOT
970 LSR SMPL
980 BCS UNE
990 INC SMPL
1000 JMP WTBUSY
1010 .UNE
1020 LDA DOTBSE
1030 SEC
1040 SBC #&08
1050 BCS TWO
1060 DEC DOTBSE+1
1070 .TWO
1080 STA DOTBSE
1090 LDA ROWBSE+1
1100 STA RWBSSH+1
1110 LDA ROWBSE
1120 STA RWBSSH
1130 SEC
1140 SBC #128
1150 BCS THREE
1160 DEC RWBSSH+1
1170 .THREE
1180 STA RWBSSH
1190 DEC RWBSSH+1
1200 DEC RWBSSH+1
1210 LDA DOTBSE+1
1220 CMP RWBSSH+1
1230 BNE WTBUSY
1240 LDA DOTBSE
1250 CMP RWBSSH
1260 BNE WTBUSY
1270 TYA
1280 PHA
1290 TXA
1300 PHA
1310 LDA #&81
1320 LDX #&00
1330 LDY #&00
1340 JSR &FFF4
1350 TYA
1360 BNE NEWLNE
1370 PLA:PLA:JMP EIGHT
1380 .NEWLNE PLA
1390 TAX
1400 PLA
1410 TAY
1420 LDA ROWBSE
1430 SEC
1440 SBC #&01
1450 INY
1460 BCS FOUR
1470 DEC ROWBSE+1
1480 .FOUR
1490 STA ROWBSE
1500 STA DOTBSE
1510 LDA ROWBSE+1
1520 STA DOTBSE+1
1530 CPY #&08
1540 BEQ SIX
1550 JMP WTSYNC
1560 .SIX
1570 LDA ROWBSE
1580 LDY #&00
1590 SEC
1600 SBC# 120
1610 BCS FIVE
1620 DEC ROWBSE+1
1630 DEC DOTBSE+1
1640 .FIVE
1650 STA ROWBSE
1660 STA DOTBSE
1670 DEC ROWBSE+1
1680 DEC ROWBSE+1
1690 DEC DOTBSE+1
1700 DEC DOTBSE+1
1710 STY SMPL
1720 LDA ROWBSE+1
1730 CMP FINSCN+1
1740 BEQ SEVEN
1750 BCC SEVEN
1760 JMP WTSYNC
1770 .SEVEN
1780 JMP EIGHT
1790 LDA ROWBSE
1800 CMP FINSCN
1810 BEQ EIGHT
1820 BCC EIGHT
1830 JMP WTSYNC
1840 .EIGHT
1850 CLI
1860 RTS
1870 ]
1880 NEXT P
1890 IF HRES>0 AND HRES<5 THEN ?(RESH+1)=HRES
1900 CALL CODE%
1910 GOTO 90
```

Program 2.

```
Hisoft GENA3.1 Assembler.

A028                10         ORG  41000
A028                20         ENT  $
F8F0                30 PORT:   EQU  #F8F0
9C40                40 TEMP:   EQU  40000
9C41                50 LUM:    EQU  40001
9C42                60 XREG:   EQU  40002
9C44                70 YREG:   EQU  40004
9C46                80 HXREG:  EQU  40006
9C48                90 BLKADD: EQU  40008
A028  3E00         100         LD   A,#00
A02A  32479C       110         LD   (HXREG+1),A
A02D  CD0EBC       120         CALL #BC0E
A030  219F00       130 RERUN:  LD   HL,159
A033  22429C       140         LD   (XREG),HL
A036  21C700       150         LD   HL,199
A039  22449C       160         LD   (YREG),HL
A03C  DD2142A1     170         LD   IX,BYTEAD+15
A040  3E0F         180         LD   A,#0F
A042  32409C       190         LD   (TEMP),A
A045  DD7E00       200 COLSET: LD   A,(IX+0)
A048  47           210         LD   B,A
A049  4F           220         LD   C,A
A04A  3A409C       230         LD   A,(TEMP)
A04D  CD32BC       240         CALL #BC32
A050  21409C       250         LD   HL,TEMP
A053  35           260         DEC  (HL)
A054  FA5CA0       270         JP   M,WTFRM
A057  DD2B         280         DEC  IX
A059  C345A0       290         JP   COLSET
A05C  CD19BD       300 WTFRM:  CALL #BD19
A05F  CD19BD       310         CALL #BD19
A062  F3           320 LOOP1:  DI
A063  01F0F8       330         LD   BC,#F8F0
A066  ED78         340 LINE:   IN   A,(C)
A068  CB77         350         BIT  6,A
A06A  28FA         360         JR   Z,LINE
A06C  ED78         370 ENLIN:  IN   A,(C)
A06E  CB77         380         BIT  6,A
A070  20FA         390         JR   NZ,ENLIN
A072  160A         400         LD   D,10
A074  15           410 DELAY:  DEC  D
A075  20FD         420         JR   NZ,DELAY
A077  F3           430 LOOP2:  DI
A078  1602         440         LD   D,2
A07A  01F0F8       450         LD   BC,#F8F0
A07D  ED78         460 SMPL:   IN   A,(C)
A07F  CB7F         470         BIT  7,A
A081  20FA         480         JR   NZ,SMPL
A083  ED78         490 ENSMP:  IN   A,(C)
A085  CB7F         500         BIT  7,A
A087  28FA         510         JR   Z,ENSMP
A089  15           520         DEC  D
A08A  20F1         530         JR   NZ,SMPL
A08C               540 GETLUM:
A08C  ED78         550         IN   A,(C)
A08E  E60F         560         AND  #0F
A090  32419C       570         LD   (LUM),A
A093  1F           580         RRA
A094  CB18         590         RR   B
A096  1F           600         RRA
A097  CB18         610         RR   B
A099  1F           620         RRA
A09A  CB19         630         RR   C
A09C  1F           640         RRA
A09D  CB18         650         RR   B
A09F  1600         660         LD   D,0
A0A1  CB00         670         RLC  B
A0A3  CB1A         680         RR   D
A0A5  CB1A         690         RR   D
A0A7  CB00         700         RLC  B
A0A9  CB1A         710         RR   D
A0AB  CB1A         720         RR   D
A0AD  CB01         730         RLC  C
A0AF  CB1A         740         RR   D
A0B1  CB1A         750         RR   D
A0B3  CB00         760         RLC  B
A0B5  CB1A         770         RR   D
A0B7  3A429C       780         LD   A,(XREG)
A0BA  1F           790         RRA
A0BB  3003         800         JR   NC,NOLFT
A0BD  B7           810         OR   A
A0BE  CB1A         820         RR   D
A0C0  32469C       830 NOLFT:  LD   (HXREG),A
A0C3  7A           840         LD   A,D
A0C4  32409C       850         LD   (TEMP),A
A0C7  210050       860         LD   HL,#5000
A0CA  3A449C       870         LD   A,(YREG)
A0CD  CB3F         880         SRL  A
A0CF  CB3F         890         SRL  A
A0D1  CB3F         900         SRL  A
A0D3  5F           910         LD   E,A
A0D4  1600         920         LD   D,0
A0D6  0608         930         LD   B,8
A0D8  29           940 MULT:   ADD  HL,HL
A0D9  3001         950         JR   NC,NOADD
A0DB  19           960         ADD  HL,DE
A0DC  10FA         970 NOADD:  DJNZ MULT
A0DE  22489C       980         LD   (BLKADD),HL
A0E1  3A449C       990         LD   A,(YREG)
A0E4  CB27        1000         SLA  A
A0E6  CB27        1010         SLA  A
A0E8  CB27        1020         SLA  A
A0EA  E638        1030         AND  56
A0EC  67          1040         LD   H,A
A0ED  2E00        1050         LD   L,0
A0EF  ED4B489C    1060         LD   BC,(BLKADD)
A0F3  09          1070         ADD  HL,BC
A0F4  0100C0      1080         LD   BC,#C000
A0F7  09          1090         ADD  HL,BC
A0F8  ED4B469C    1100         LD   BC,(HXREG)
A0FC  09          1110         ADD  HL,BC
A0FD  3A409C      1120         LD   A,(TEMP)
A100  DD21429C    1130         LD   IX,XREG
A104  DDCB0046    1140         BIT  0,(IX+0)
A108  2001        1150         JR   NZ,PLOT
A10A  B6          1160         OR   (HL)
A10B  77          1170 PLOT:   LD   (HL),A
A10C  010100      1180         LD   BC,#0001
A10F  2A429C      1190         LD   HL,(XREG)
A112  B7          1200         OR   A
A113  ED42        1210         SBC  HL,BC
A115  3806        1220         JR   C,NEXY
A117  22429C      1230         LD   (XREG),HL
A11A  C377A0      1240         JP   LOOP2
A11D  219F00      1250 NEXY:   LD   HL,159
A120  22429C      1260         LD   (XREG),HL
A123  2A449C      1270         LD   HL,(YREG)
A126  B7          1280         OR   A
A127  ED42        1290         SBC  HL,BC
A129  3002        1300         JR   NC,NEWLIN
A12B  FB          1310         EI
A12C  C9          1320         RET
A12D  22449C      1330 NEWLIN: LD   (YREG),HL
A130  C362A0      1340         JP   LOOP1
A133              1350 BYTEAD:
A133  00010204    1360         DEFB 0,1,2,4
A137  0506080A    1370         DEFB 5,6,8,10
A13B  0C0E1012    1380         DEFB 12,14,16,18
A13F  1416181A    1390         DEFB 20,22,24,26

BLKADD 9C48   BYTEAD A133   COLSET A045
DELAY  A074   ENLIN  A06C   ENSMP  A083
GETLUM A08C   HXREG  9C46   LINE   A066
LOOP1  A062   LOOP2  A077   LUM    9C41
MULT   A0D8   NEWLIN A12D   NEXY   A11D
NOADD  A0DC   NOLFT  A0C0   PLOT   A10B
PORT   F8F0   RERUN  A030   SMPL   A07D
TEMP   9C40   WTFRM  A05C   XREG   9C42
YREG   9C44

Table used:    307 from    350
Executes: 41000
```

Program 3.

```
5 MEMORY 30000:MODE 2
10 LOAD"wefax1.obj"
20 INPUT"enter horizontal resolution 1-4";resh
30 IF resh>0 AND resh<5 THEN POKE &A079,
resh ELSE CLS:GOTO 20
40 CALL 41000
50 CALL &A030
60 GOTO 50
```

SATELLITE DECODER PARTS LIST

RESISTORS: All 0.6W 1% Metal Film

R1	27k	1	(M27K)
R2,4,25	470k	3	(M470K)
R3,37,38,39,40	1k	5	(M1K)
R5,9,20,27	10k	4	(M10K)
R6,7,12,24	100k	4	(M100K)
R8	820Ω	1	(M820R)
R10	220k	1	(M220K)
R11,17,26	2k2	3	(M2K2)
R13	180k	1	(M180K)
R14,41	47k	2	(M47K)
R15	5k6	1	(M5K6)
R16,21,22,23,28, 30,31,34,35,36	4k7	10	(M4K7)
R18	180k	1	(M180K)
R19	390Ω	1	(M390R)
R29	330Ω	1	(M330R)
R32,33	270Ω	2	(M270R)
SIL 1,2	SIL 4k7	2	(RA29G)
RV1	10k Cermet	1	(WR42V)
RV2	1k Hor. S-Min Preset	1	(WR55K)
RV3	10k Pot Lin	1	(FW02C)
RV4	1k Pot Lin	1	(FW00A)
RV5	1M Pot Lin	1	(FW08J)

CAPACITORS

C1-3	220nF Poly Layer	3	(WW45Y)
C4,5	10µF 16V Minelect	2	(YY34M)
C6,11	47nF Poly Layer	2	(WW37S)
C7	100µF 25V P.C. Electrolytic	1	(FF11M)
C8,26,27	4µ7F 35V Minelect	3	(YY33L)
C9	2µ2F 63V Minelect	1	(YY32K)
C10	2n2F Poly Layer	1	(WW24B)
C12	4n7F Poly Layer	1	(WW26D)
C13-18,28	100nF Minidisc	7	(YR75S)
C19-22	2200µF 35V Axial Electrolytic	4	(FB90X)
C23	10µF 16V Tantalum	1	(WW68Y)
C24,25	100nF Polyester	2	(BX76H)

SEMICONDUCTORS

D1,2	OA91	2	(QH72P)
D3-14	1N4148	12	(QL80B)
ZD1	BZY88C3V3	1	(QH02C)
LED 1	Red LED Chrome large	1	(YY60Q)
LED 2	Green LED Chrome large	1	(QY47B)
TR1-3	BC548	3	(QB73Q)
BR1	W005	1	(QL37S)
REG1	µA7912UC	1	(WQ93B)
REG2	µA7812UC	1	(QL32K)
REG3	µA7805UC	1	(QL31J)
IC1	LF353	1	(WQ31J)
IC2	ZN427E	1	(UF40T)
IC3	NE565	1	(WQ56L)
IC4	74LS132	1	(YF51F)
IC5	4078	1	(QX28F)
IC6-8	74HC163	3	(UB42V)
IC9	74LS03	1	(YF03D)

MISCELLANEOUS

M1	Signal Meter	1	(LB80B)
T1	Transformer Toroidal 30VA 15V	1	(YK11M)
S1	Switch Sub. Min. Toggle SPDT (C)	1	(FH02C)
S2,4	Switch Rotary 3-pole 4-way	2	(FF75S)
S3	Switch Sub-Min Toggle SPDT (D)	1	(FH03D)
S5	Switch Dual Rocker Neon	1	(YR70M)
FS1	Fuse 1A A/S	1	(WR19V)
PL1,3	Minicon latch Plg 2-Way	2	(RK65V)
PL2	Minicon latch Plg 12-Way	1	(YW14Q)
PL4	Minicon latch Plg 6-Way	1	(YW12N)
PL5,6	Minicon latch Plg 8-Way	3	(YW13P)
PL7	R.A. 'D' Range 25-Way PCB Plg	1	(FG68Y)
SK1,3	Minicon latch Housing 2-Way	2	(HB59P)
SK2	Mincon latch Housing 12-Way	1	(YW24B)
SK4	Minicon latch Housing 6-Way	1	(BH65V)
SK5,6	Minicon latch Housing 8-Way	3	(YW23A)
	Minicon Terminal	46	(YW25C)
SK8	6-Pin PCB DIN Socket	1	(FA90X)
SK9	Power Socket D.C. 2.5mm	1	(FK06G)
SK10-12	2x12-Way P.C. Edgeconn	3	(BK74R)
	Polarising Key 0.156in	3	(FD08J)
	Bolt 6BA x 1in	1 Pkt	(BF07H)
	6BA x ¼in Threaded Spacer	1 Pkt	(FD10L)
	Nut 6BA	1 Pkt	(BF18U)
	Tag 2BA	1 Pkt	(BF27E)
	Bolt 6BA x ½in	1 Pkt	(BF06G)
	Mains Warning Label	1	(WH48C)
	Cable Min Mains White	1 mtr	(XR02C)
	Ribbon Cable 20-Way	1 mtr	(XR07H)
	Grommet Small	1	(FW59P)
	S.R. Grommet 6W-1	1	(LR49D)
	Sleeving Heatshrink CP95	1 mtr	(YR17T)
	Clip-on TO220 Heatsink	1	(FG52G)
	Decoder PCB	1	(GD22Y)
	Veropin 2141	1 Pkt	(FL21X)
	DIL Socket 8-pin	1	(BL17T)
	DIL Socket 14-pin	4	(BL18U)
	DIL Socket 16-pin	3	(BL19V)
	DIL Socket 18-pin	1	(HQ76H)
	Safuseholder 20	1	(RX96E)
	Knob K10B	5	(RK90X)
	Transformer Mounting Bracket	1	(FD09K)
	Constructor's Guide	1	(XH79L)

OPTIONAL

	Instrument Case NM2H	1	(YM51F)
	Decoder Front Panel	1	(FD05F)
	Araldite	1	(FL44X)
	DIN Plug 6-pin	2	(HH29G)
	Standard Power Plug 2.5	2	(HH62S)
	Cable Single Core Screened Grey	1 mtr	(XR13P)
	Multi-Core 6-Way	1 mtr	(XR26D)
	Decoder Interface Cable	1	(FD17T)

A complete kit of all parts, excluding optional items, is available for this project:
Order As LM07H (MAPSAT Decoder Kit)
The following items included in the above kit list are also available separately, but are not shown in the 1986 catalogue:
Sub-Min Toggle SPDT **Order As FH02C**
6-Pin PCB DIN Socket **Order As FA90X**
0.156in Edgeconn Polarising Key **Order As FD08J**
¼in x 6BA Threaded Spacer **Order As FD10L**
Decoder PCB **Order As GD22Y**
MAPSAT Decoder Front Panel **Order As FD05F**
Transformer Mounting Bracket **Order As FD09K**
Instrument Case NM2H **Order As YM51F**
Decoder Interface Cable **Order As FD17T**
Constructor's Guide **Order As XH79L**

DECODER SYNC TONE BOARD PARTS LIST

RESISTORS: All 0.6W 1% Metal Film

R1	2k2	1	(M2K2)
R2,10,11,13,22	47k	5	(M47K)
R3	100k	1	(M100K)
R4-7	33k	4	(M33K)
R8,9	470k	2	(M470K)
R12	68k	1	(M68K)
R14	82k	1	(M82K)
R15	18k	1	(M18K)
R16,19	220Ω	2	(M220R)
R17,18,20,21	4k7	4	(M4K7)
R23	220k	1	(M220K)
R24	2k7	1	(M2K7)
RV1,2	47k Vert S. Preset	2	(WR70Q)
RV3-5	10k 23-Turn Cermet	3	(WR49D)

CAPACITORS

C1,2,5,6	100nF Poly Layer	4	(WW41U)
C3	2n2F Poly Layer	1	(WW24B)
C4	10nF Poly Layer	1	(WW29G)
C7	100µF 16V Minelect	1	(RA55K)
C8	10µF 16V Minelect	1	(YY34M)
C9,10	220nF Poly Layer	2	(WW45Y)

SEMICONDUCTORS

D1-3	1N4148	3	(QL80B)
TR1-3	BC548	3	(QB73Q)
IC1	4046BE	1	(QW32K)
IC2	MF10CN	1	(QY35Q)

MISCELLANEOUS

	Veropin 2145	1 Pkt	(FL24B)
	Sync 1 PCB	1	(GD23A)
	Track pin	1 Pkt	(FL82D)
	DIL Socket 20-Pin	1	(HQ77J)

A complete kit of all parts is available for this project:
Order As LM08J (Decoder Sync Tone Kit)
The following item in the above kit list is also available separately, but is not shown in the 1986 catalogue:
Sync 1 PCB **Order As GD23A**